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Final Technical Report
March 1980

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LEVEL II

MODULAR C 3 INTERFACE ANALYSIS (FLEXIBLE INTRACONNECT) Study Methodology and Results

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This report documents the results of the concept definition phase for a high capacity wideband general purpose data/communications bussing system. A "Flexible Intraconnect" bus concept is described in terms of its use to achieve physical and functional modularity in the design, implementation and operational deployment of command and control (C^2), centers of the Tactical Air Force (TAF). Flexible Intraconnect (FI) design parameters are established in terms of traffic loading estimates and

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requirements of evolving configurations of C^2 centers of the TAF. Surveys of data distribution system architectures, current and developing technologies and C^2 device interfaces are provided. A design of a Flexible Intraconnect having high data rate and capacity, positive flow control and configuration flexibility is documented. A standardized interface for physical and functional device to bus access is described. Descriptions of the major functional elements of the FI are provided along with top level block diagrams. The design was analyzed and preliminary estimates of error performance, reliability, capacity and response times were derived. Results obtained from this phase will be used in specifications for the subsequent development phase of the FI program.

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PART 1
INTRODUCTION AND SUMMARY

Part 1 – Introduction and Summary

1. REQUIREMENTS FOR A MODULAR C^3 FLEXIBLE INTRACONNECT

A new method for connecting devices, subsystems, and centers is required in order to achieve a truly modular approach to the operational needs of the Tactical Air Force.

Current Tactical Air Force C^3 Centers are characterized by designs which are tailored or custom-made for a specific set of operational requirements and equipment characteristics. While these designs provide the performance characteristics identified as necessary at the time of conception, the design approach had inherent limitations (due to the technology available) which restricted flexibility, adaptability, deployability, growth, and interoperability.

A solution to these limitations is the development of modular elements in each of three system segments: hardware, software, and connecting links. The goals of such a modular concept would include:

- The ability to configure a wide variety of functionally different centers
- The ability to assemble a wide variety of center sizes
- The capability of introducing new devices in the field as they are developed, without center redesign or modification
- The capability for the center commander to reconfigure or reallocate tasks and functions in the field in order to meet a changing environment
- The ability to re-implement present day centers.

Recent technology advancements have made the development of a cost effective modular design, achieving the goals listed above, feasible and timely. Key areas of the new technology are microprocessors, LSIs, and fiber optics.

The Modular C^3 Flexible Intraconnect Analysis is aimed at providing a concept for one of the three segments -- hardware, software, connecting links – that comprise a modular C^3 design.

In order for the modular C^3 concept to be successful, the intraconnect design must strive to reach the same goals as other modular C^3 elements. Therefore a first step in developing the intraconnect concept is the establishment of specific characteristics and features which, if satisfied by the flexible intraconnect design, would indeed satisfy these goals. The key specific flexible intraconnect requirements are listed in the table. Some were defined in the statement of work, others were defined during the course of the study.

TABLE 1.1-1. FLEXIBLE INTRACONNECT DESIGN REQUIREMENTS

- Provide the transmission capacity necessary to support present data rates and those expected in the 1990 time frame.
- Transfer data via a method which is transparent to the contents of the data being exchanged by intraconnect users.
- Provide a standard interface so that present and future devices – both simple and complex – can be tied into the net.
- Provide for "sub-networks" for the exclusive use of groups of designated devices.
- Provide for on-line, but not dynamic, reconfiguration of user devices.
- Provide self-checking capabilities and support security needs of users.
- Transmit data over a 5 mile range.
- Interface with existing communications subsystems such as TCCF microwave, troposcatter, and satellite.

2. OVERVIEW OF THE FLEXIBLE INTRACONNECT

The Star/Bus Flexible Intraconnect, developed in this Mod C^3 Interface Analysis, provides for all known present and planned Tactical Air Force C^3 Center configuration and information exchange requirements. Because of its inherent flexibility, it is adaptable to the forseeable growth and interoperability needs of the future.

In an intensive study, analysis, and design effort, over a period of 17 months, Hughes and the Government in a joint effort, developed a Flexible Intraconnect (FI) concept and preliminary design for interconnecting the devices, facilities, and shelters of Tactical Command and Control Centers. The FI as it is referred to throughout this report, is designed with the flexibility to meet current, planned, and future requirements as they are projected to evolve from today to the post 1990 time frame. This design was accomplished by an interdisciplinary team of technical and operational specialists, iteratively developing the FI design in a three task effort: 1) developing an FI design concept, 2) analyzing FI interfaces, and 3) developing a preliminary FI design. A major part of the effort involved analyzing the configurations and operations of existing and planned TAF C^3 Centers, studying the TAFIIS Master Plan, developing current and potential requirements for the FI, and verifying the design results

An exhaustive survey of data distribution system architectures and device technologies, and a thorough analysis of potential user device interfaces were performed. This resulted in the development of an FI design providing a high data rate and connectivity capacity, positive flow control, and configuration flexibility in a Star/Bus hierarchial topology. In addition, a standard interface for connecting C^3 devices to the intraconnect was developed.

The FI can be described in terms of its architectural components: topology, protocol, and media. The FI design applies to single facility as well as multi-facility centers. Figure 1.1-1 illustrates the FI architecture applied to a five shelter C^3 center. The shelters may be colocated or dispersed over a wide area. The star/bus topology provides for star connection of clustered equipments to the Local Intraconnect (LI), a concentrated 90 Mb/s TDMA bus. The LIs located near clustered equipments within a single facility center (or within shelters of a multi-operations-module center) are interconnected by the External Intraconnect (EI) which is a distributed TDMA bus on fiber optic cables. As a result, all devices, in all shelters on the FI are virtually interconnected. Double lines are shown in the figure to symbolize a transmit bus and a receive bus harmonized to provide efficient propagation time compensation. Point-to-point fiber optic connections with three 20 Mb/s fibers per bus result in 60 Mb/s EI capacity. To increase survivability of the system a passive fiber-optic cable bypass capability is provided at each shelter to allow FI operation to continue in the event of shelter losses.

The protocol of data transfer control on the LIs and the EI is a time slotted reservation system on a TDMA bus. Although the protocols are generally the same, there are differences between the Local and External Intraconnects based on their physical structures and control mechanisms. For example, even though each Local intraconnect and External Intraconnect operates within itself as a synchronous TDMA bus, they are not synchronized with each other. That is, they are asynchronous with respect to each other. Also, the potentially dispersed External Intraconnect operates with distributed control between shelters, but the concentrated Local Intraconnect

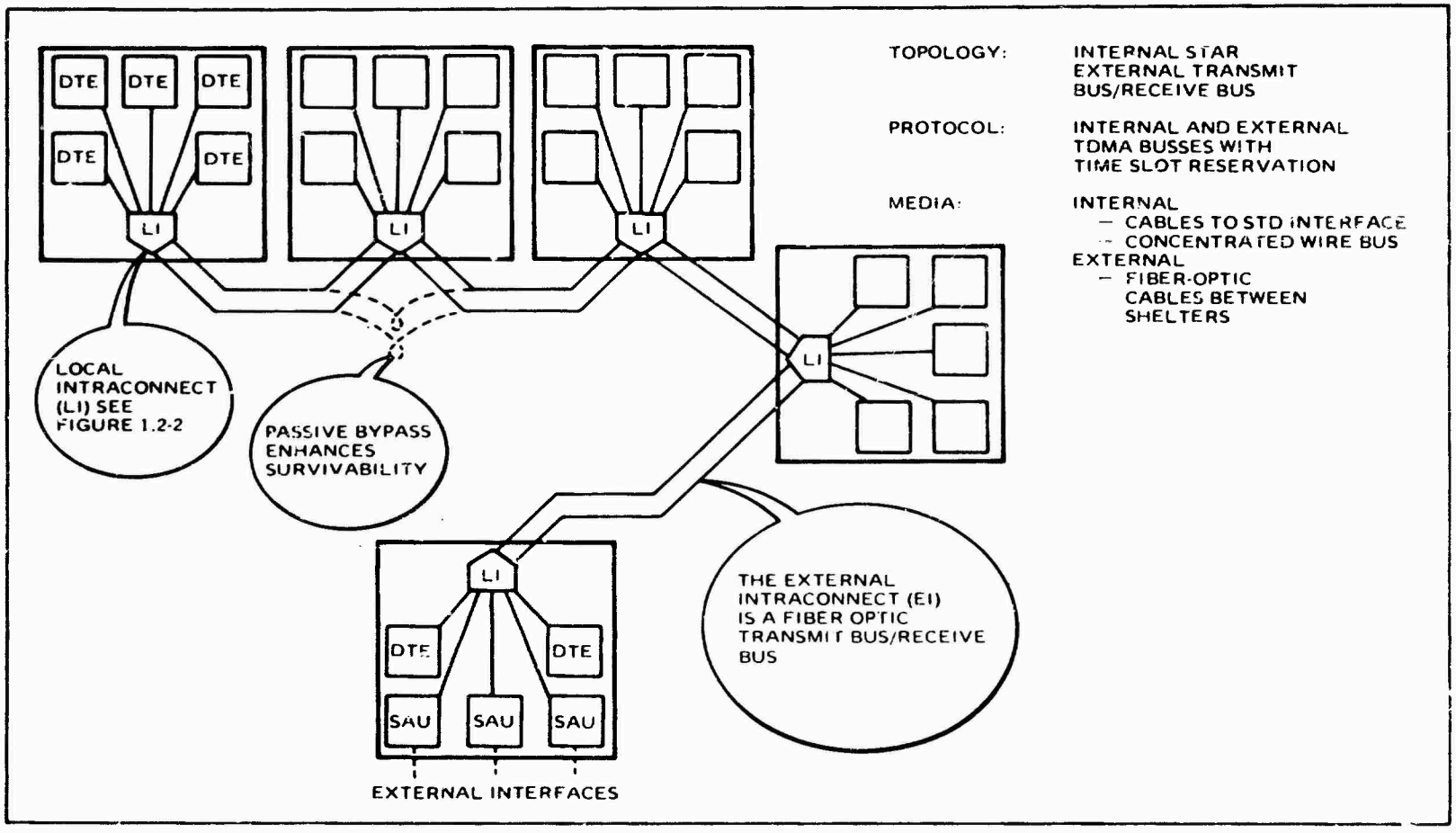

Figure 1.2-1. System Overview of the Flexible Intraconnect. The star/bus architecture optimizes the FI design for clustered C^3 devices and widely dispersed shelters.

2. OVERVIEW OF THE FLEXIBLE INTRACONNECT (Continued)

operates with central control. The Star/Bus combination provides for both survivability and efficiency, by optimizing for typical center topologies.

The Local Intraconnect (based on a TDMA concept developed in Task I) is a concentrated (inches long) set of 18 parallel TDMA busses operating at a nominal 5 Mb/s which results in a total capacity of 90 Mb/s (see Figure 1.2-2). Local Intraconnect Units provide buffer and control interfaces to the Device Terminal Equipments (DTE) with standard interfaces. The Preferred Standard Interface (PSI) has versatile positive control (implemented in a simple physical structure) and is ideal for all future command and control devices. In a shelter application, the standard interface would be available at standard receptacles distributed appropriately on the internal shelter walls, for convenient connection of devices to the local intraconnect. Selected Adapter Units (SAU), convert non-standard interfaces to the PSI, providing for operation with existing and other devices. The External Intraconnect Unit (EIU) provides the asynchronous buffering and gating between the Local and External Intraconnects. A Local Intraconnect Control Unit (LICU) provides timing, configuration, and reservation control for the LI. Special signals, such as analog signals, may be provided for by digitizing them in an SAU and handling them in the FI as data messages, or they may be handled in separate channels via an Analog Interface Unit (AIU). A Shelter-Shelter Unit (SSU) provides for direct connection between shelters or facilities not otherwise connected by the external intraconnect. The AIU and SSU functions were identified in Task I, but were not analyzed further. Task II and III analyses concentrated on digital data distribution via the Preferred Standard Interface, Local Intraconnect and External Intraconnect.

The FI design provides for three basic types of messages: Block, Virtual Bus, and Lazy Susan.

- Block Messages – Variable length messages (up to 1024 words) either broadcast or discrete addressed.
- Virtual Bus Messages – Variable length messages broadcast to all members of the bus.
- Lazy Susan Messages – Variable length messages transmitted in a predetermined sequence to members of the bus. (e.g., User 1 to User 4; User 4 to User 2; User 2 to User 3; User 3 to User 1).

In the EI, Block messages are of two types. A Short Block (SB) message has been implemented in order to make use of propogation delay times. The Short Block messages are limited to messages shorter than 64 words.

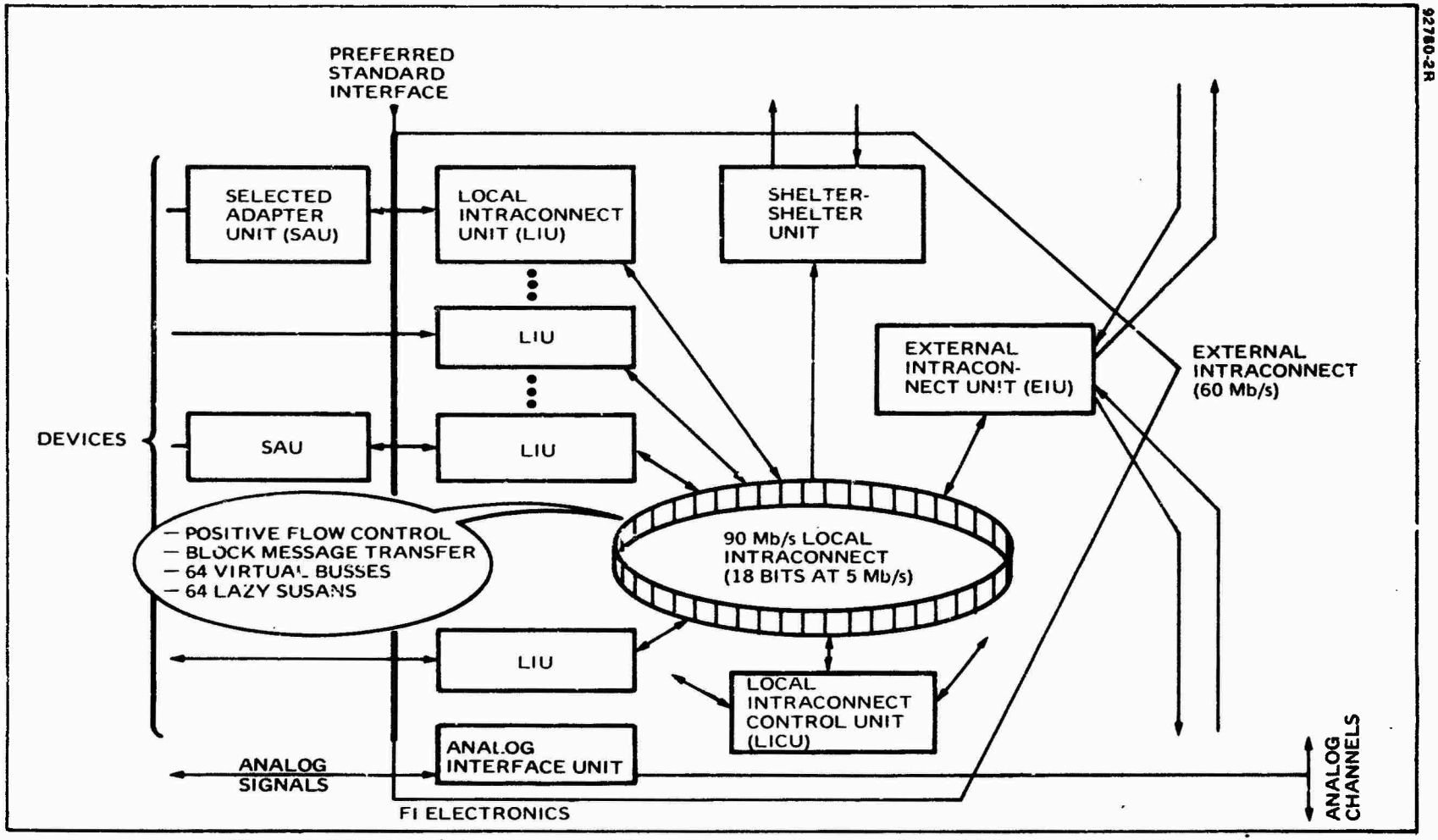

Figure 1.2-2. Local Intraconnect. A concentrated bus provides a high capacity and low risk transmission medium for clustered devices.

PART 2
SUMMARY OF TASK I, CONCEPTUAL DESIGN ANALYSIS

Part 2 – Summary of Task 1 – Conceptual Design Analysis

1. CONCEPTUAL DESIGN METHODOLOGY

A series of highly interactive analyses enabled development of the most cost effective conceptual design for a Mod C^3 Flexible Intraconnect architecture.

Past TAF C^3 systems have been developed to meet a limited set of operational requirements and are so optimized for those requirements that they may not operate together effectively with functionally related systems. In addition, they are characterized by high life cycle costs and long lead times from validation of requirements to initial operating capability. Microelectronic technology and interconnect techniques have progressed to the point where standard modules, a flexible connection architecture and a standard interface can be employed to integrate the elements of individual tactical C^3 system. Element modularization would support the development of flexible systems and the reduction of design, procurement and operating costs. One of the key elements needed to realize these goals is the development of a flexible connection scheme which has a common interface standard that can be effectively integrated into existing systems and applied to future systems as well. Therefore, the purpose of the Task 1 effort was to develop a flexible modular concept for the connecting devices, shelters and functions which comprise a tactical C^3 system.

This flexible intraconnect should provide operational users the flexibility to meet current, projected and future requirements. It should promote interoperability of centers as well as equipments and it should not compromise presently employed functional relationships and operational procedures.

Four major analyses were performed to arrive at a most cost-effective Flexible Intraconnect design concept. They were (Figure 2.1-1) an analysis of configuration alternatives, a functional information flow analysis, a technology review and design concept development analysis, and a weighted rating trade analysis of the design concepts. Because of the limited schedule available for the analyses, teams were formed to address the individual issues, in as parallel and simultaneous a manner as possible. There was significant iteration and cooperation between the teams and the analyses tasks.

The analysis of the configuration alternatives task consisted of a survey of existing and planned TACS C^3 centers, and an analysis of the TAFIIS Master Plan, in order to develop four System Configuration Concepts (SCCs). Functional information flow analysis was performed on these concepts to develop equipment connectivity and data distribution loading requirements for the Flexible Intraconnect.

In an overlapping effort design engineers surveyed existing and developing technologies which could impact the FI design, and developed several candidate approaches for FI designs, emphasizing interconnectivity, flexibility, modularity, interoperability and survivability. These approaches were then overlayed on TACS C^3 center configurations, applying the developed load and connectivity requirements to test the candidate concept. Iterations of

the above process refined and narrowed the candidate FI concepts to six candidates based on three fundamental approaches. The six candidates were then subjected to an evaluation process that involved a weighted rating trade analysis, combined with cost, sensitivity and consistency analyses, to select the most cost-effective FI Design Concept.

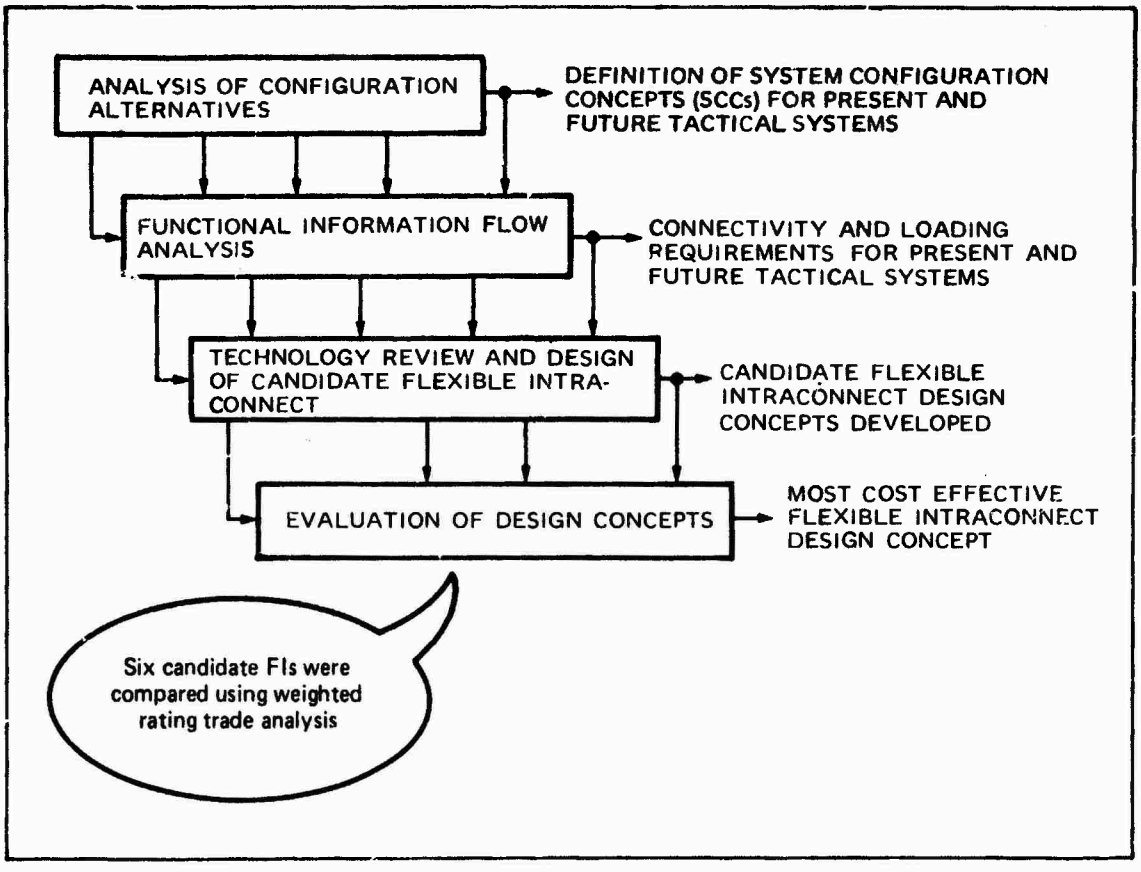

Figure 2.1-1. Overview of Study Approach. Multidisciplined analysis went into the development and selection of the optimum FI concept.

Part 2 – Summary of Task I, Conceptual Design Analysis

2. ANALYSIS OF CONFIGURATION ALTERNATIVES

Four sets of TACS C^3 centers were defined and used as a basis for developing and evaluating the candidate conceptual FIs.

The TAFIIS Master Plan was used as the primary source document to develop the present, near term and future TACS systems. Four System Configuration Concepts (SCCs) as shown in Table 2.2-1 were postulated, to represent the present Air Force TACS, the near term automation of some of the TACS elements, and two future (1985-1990) systems.

The SCC-1 represents the present 407L System which is primarily a manual system. The CRCs and CRPs are automated and pass digital track data among themselves. All other centers were considered to be manual (FACP, TACC, DASC, ALCC, etc.) with track data being passed by voice, and other operational data being transmitted/received by teletype and facsimile.

The SCC-2 is a postulated upgrading of the 407L System in consonance with the objectives of the TAFIIS Master Plan. The TACC was separated into two centers (operations and plans) and incorporated the appropriate intelligence functions into each. The FACP was assumed to be automated and interconnected with the CRCs/CRPs for the passage of digital track data. All other centers were manual, with teletype and facsimile located in the appropriate centers.

The SCC-3 was developed as one of two alternative systems for the 1990s. The anticipated highly mobil threat in the European environment and the rapid advance in automation technology indicated that TACS netting and rapid dissemination of tactical information was essential for survivability and to counter the threat. Therefore, all TACS systems were automated with the additional capability to pass high resolution photography, video and graphic displays digitally from center to center as may be required. The teletype and facsimile capability was retained where it was employed by TACS centers in the SCC-2 configuration. An essential difference in SCC-3 over the previous SCCs, was that centers were now shelterized in either 8x8x20 foot or 8x8x10 foot shelters to provide centers greater mobility. Each center was reviewed to determine the essential manpower requirements (based on Tactical Air Control Manuals, TACM 55-44 and 55-45) to perform the requisite operational functions. Based on these functions, the numbers and types of shelters per center were assigned, and numbers and types of data processing equipments were assigned to each shelter. These configurations were used in the next task.

SCC-4 was an alternative to SCC-3. Because of the anticipated high density, highly mobil threat, the FACPs were increased and given greater operational autonomy. This was possible through the concept of centralized control and supervision, but with delegation of greater responsibilities for execution to lower echelons (FACPs). The greater number of FACPs nearer the FEBA allowed for rapid setup and teardown to move, relocate and be on the 'air' to counter the enemy threat. In conjunction with the increase of FACPs (truck mounted and mobil) the CRCs were deleted from the TACS. Another minor change in the concept was the decrease in the number of large shelters (such as

at the TACC operations and plans centers). This latter change had no significant effect on the FI loading.

A large force deployment, as specified in TACM 55-45, was used to determine the total number and type of TACS centers. Therefore, it was a development task to arrive at a force strength that was realistic and would serve to bound the high level of traffic in a high density combat environment.

TABLE 2.2-1. SYSTEM CONFIGURATION CONCEPTS

Four SCC's represent a postulated set of evolutionary TACS C^3 centers from today through the 1990's.

SCC-1	Primarily manual, todays TACS. The CRCs and CRPs are automated.
SCC-2	Upgrading of 407L. The TACC is split into 2 centers with the appropriate intelligence personnel functions incorporated. The FACP is automated.
SCC-3	All TACS centers are automated and equipped with a family of standardized shelters for greater mobility. The capability exists for digital passage of high resolution photography, video and graphic displays.
SCC-4	The same as SCC-3 except the number of FACPs were increased and the CRCs were deleted.

Part 2 – Summary of Task I, Conceptual Design Analysis

3. FUNCTIONAL INFORMATION FLOW ANALYSIS

Data load and intracenter connectivity analysis, which were highly interactive with the SCC definition task, provided clear insight into capacity and topology requirements of the Flexible Interconnect.

Figure 2.3-1 depicts the methodology used to derive the load at each TACS center. Estimates of the FI load for each center, for each SCC were derived. The data load for each category (shown in the box) was obtained and kept separate for traceability and sensitivity analysis.

Personnel with extensive experience in tactical air operations reviewed each center for all four SCCs and used judgements to obtain the data loads. The TAFIIS Master Plan and other GFI documentation provided guidance as to data originating centers, receiving centers, and data rates, particularly for high resolution photography and video. The latest versions (available to Hughes Aircraft Company) of the Tactical Air Control Manuals (TACM) were used to man the various centers. A high intensive threat (over 2,000 hostile and friendly aircraft) was used to derive the digital track load.

The SCC-1, being mainly a manual system, derived the FI load at each center for digital track data (TADIL B rates), teletype, facsimile, and digitized voice (16 Kb/s). The total load was derived for traffic coming into each center and for traffic leaving each center. Traffic consisted of inter-TACS traffic as well as traffic to other agencies (USA, USN, AWACS, etc.). For example, at the TACC (operations) the total number of track messages told from the CRCs was estimated. Other incoming and outgoing voice messages were estimated by operator position. Additionally, the voice time on the Intercommunications System circuit was estimated. When doubt occurred as to whether an operator would be talking, it was assumed that he would be, therefore insuring that the maximum instantaneous peak load would be obtained to determine the FI capacity requirements.

The SCC-2 is almost the same as SCC-1 except for the automated TACC (Operations and Plans) and the FACPs. The data obtained for the other centers in SCC-1 were used for the loading in SCC-2. Since the TACC and FACPs were automated, and manned differently, new loading sheets were derived. The digital traffic between the TACC and the CRCs and between the FACPs and CRPs was taken into consideration, which reduced the voice told track messages.

SCC-3 saw the introduction of digital transmission of high resolution photography, video and graphic displays. As a result, new data sheets had to be derived for each center.

SCC-4 deleted the CRCs from TACS and reduced the number of shelters at the TACC. This had little effect on the total traffic load. The number of FACPs were increased but had no significant impact on the capacity of the FI

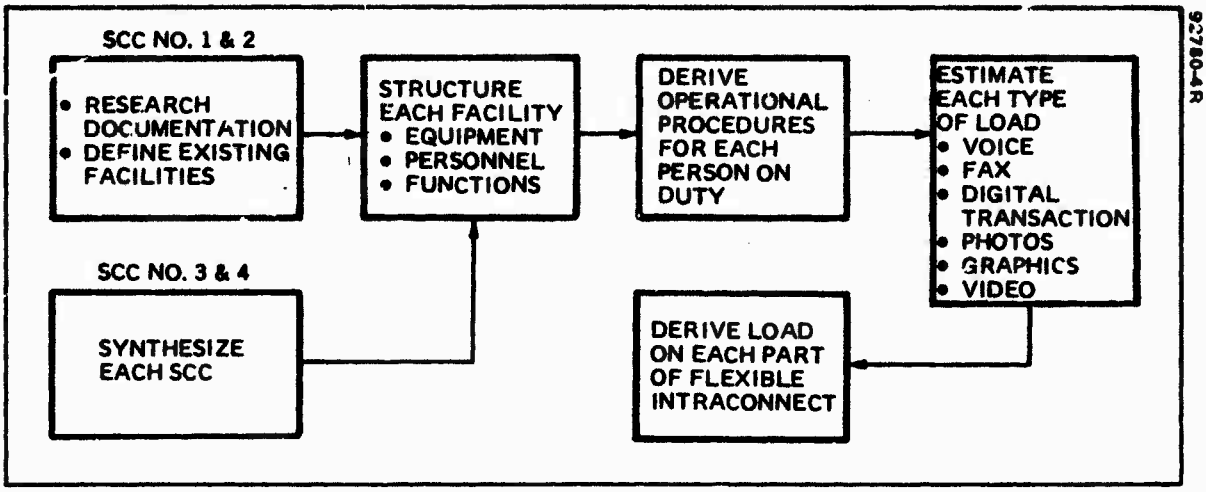

Figure 2.3-1. Connectivity Analysis Diagram. The methodology used to determine the FI loading for each of the four SCCs.

3. FUNCTIONAL INFORMATION FLOW ANALYSIS (Continued)

Figure 2.3-2 shows the data loading on various segments of the FI in a representative TACC (Operations) for SCC 3. This Center in the SCC-3 configuration is the heaviest load situation of all TAC Centers in all SCCs. The configuration is based on a shelter concept postulated by Hughes. The shelters are Self Contained (SC), Data Processing (DP), Display (DISP) and Communications (COMM).

The greatest load is on the external FI (27,253 Kb/s) which connects all of the shelters. The load within each shelter exceeds 15,000 Kb/s except for the DP shelter. The major contributor to the 15,000 Kb/s load is high resolution photography (11,500 Kb/s).

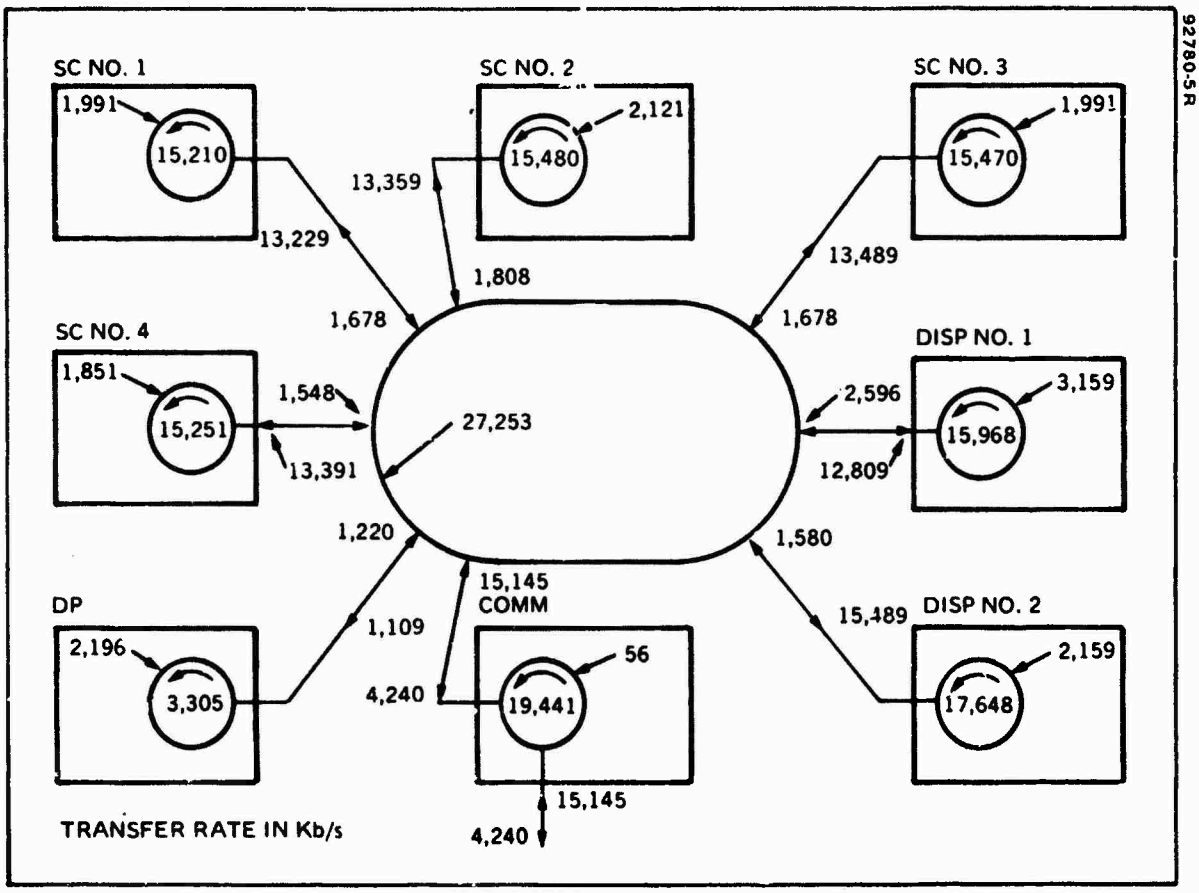

Figure 2.3-2. The TACC (Operations) FI Loading for SCC-3. The results of the analysis are shown for the TACC (Operations) SCC-3.

4. CANDIDATE FLEXIBLE INTRACONNECT DESIGNS

A limited set of candidate FI design approaches were identified via a filtering process based on load/connectivity analyses, technology reviews and government guidance. These concepts were then iteratively refined as a prelude to final concept selection.

As shown in Figure 2.4-1, the approach to developing Flexible Intraconnect design concepts was to determine requirements for the FI, review applicable technologies for implementation options, develop FI design approaches, overlay them on C^3 centers, and refine the approaches to develop six FI design concepts as candidates for evaluation and final selection. After the basic FI requirements were developed, the initial survey of technologies completed, and a few basic design approaches identified, the design team splintered into task teams developing three basic design approaches into six FI design concepts. The task teams operated in parallel, but continuously shared results, permitting the FI design candidates to be developed consistent with a common set of requirements and to benefit from a synergistic, competitive environment.

Load, connectivity and operational requirements for large and small centers, operating today and in the future were derived from the system configuration concept analyses, providing the range of requirements which dictated capacity and connectivity flexibility in the design. The Statement of Work set goals of modularity, flexibility, interoperability, connectivity and survivability, and also identified techniques of data distribution and routing. Government representatives contributed to the team effort by interpreting, modulating and refining requirements at In-Progress Reviews (IPR), as the analyses and designs progressed.

In order to develop viable approaches for the FI design concept it was necessary to review existing and developing technologies which might apply. This included data distribution system architectural components, as well as devices which might be used in the design. Architectural components included (1) topologies, such as star, bus, ring, and lattice networks, (2) protocols such as TDMA, packet switch, polling, contention, and reservation (3) media such as twisted pair, coaxial cable, fiber optic cable and microwave. Device technology developments investigated included microprocessors, surface acoustic wave devices, and charge coupled device memories. As FI design concepts developed, needs for more technology data also developed, resulting in an almost continuous technology investigation as an iterative part of the design process.

Since the number of possible architectural combinations of topology, protocol, and media initially considered was an unmanageable number to formally evaluate or develop, a preliminary filtering process was applied, eliminating impractical combinations and obvious mismatches for the C^3 application. Remaining approaches were analyzed in preliminary concept analyses

and compared with the center requirements. These were discarded, modified or refined, in an iterative process, until three basic approaches were settled on for further development. The approaches are categorized as follows: (1) distributed bus approaches including base-band and carrier operated buses, (2) concentrated bus approaches including TDMA switch, and store-and-forward techniques, (3) advanced technology approaches, characterized by very high data capacities. The candidate designs, as they developed, took advantage of all of the design approach development results. For example, some of the lessons learned in the advanced technology approach were applied to candidates using the TDMA switch, and distributed bus approaches. (In fact this may have been the major benefit of developing the advanced technology approach.)

Six candidate design concepts resulted from this "friendly" competition within the project (see Figure 2.4-2). They were (1) the multiple star concept, utilizing a TDMA microbus in each shelter and point-to-point connection between shelters; (2) A star/bus concept which had a TDMA microbus in each shelter but using a distributed Frequency Division Multiplexed (FDM) bus between shelters; (3) A star/bus concept with a TDMA microbus in each shelter but using base-band TDMA for data on a distributed bus between shelters. (FDM channels were applied for other informational uses.) (4) A bus/bus concept, utilizing a distributed data bus internal in each shelter and a distributed data bus between shelters. Both buses are base-band TDMA for data distribution and the external bus also uses FDM channels for other information. (5) A bus/bus concept, with base-band implementation for data on the internal buses but FDM carrier operation on the external bus. (6) The advanced technology FI concept, utilizing concentrators in each shelter and a distributed bus between shelters, operating at a nominal 150 Mb/s base-band data rate.

The six candidates were then subjected to a formal evaluation in order to select the most-cost-effective FI design concept. That evaluation process is described in the next topic.

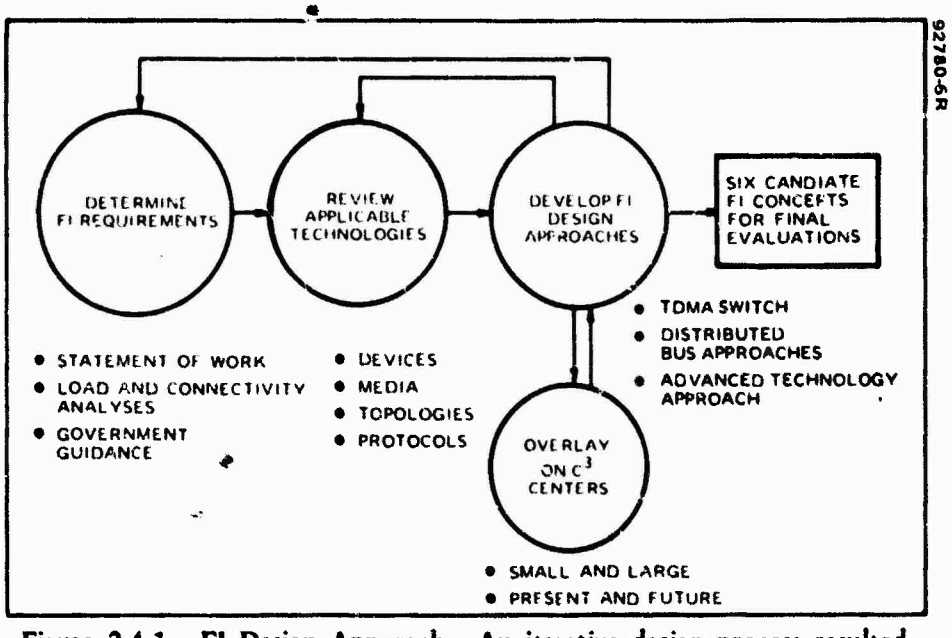

Figure 2.4-1. FI Design Apporach. An iterative design process resulted in the development of six candidate concepts.

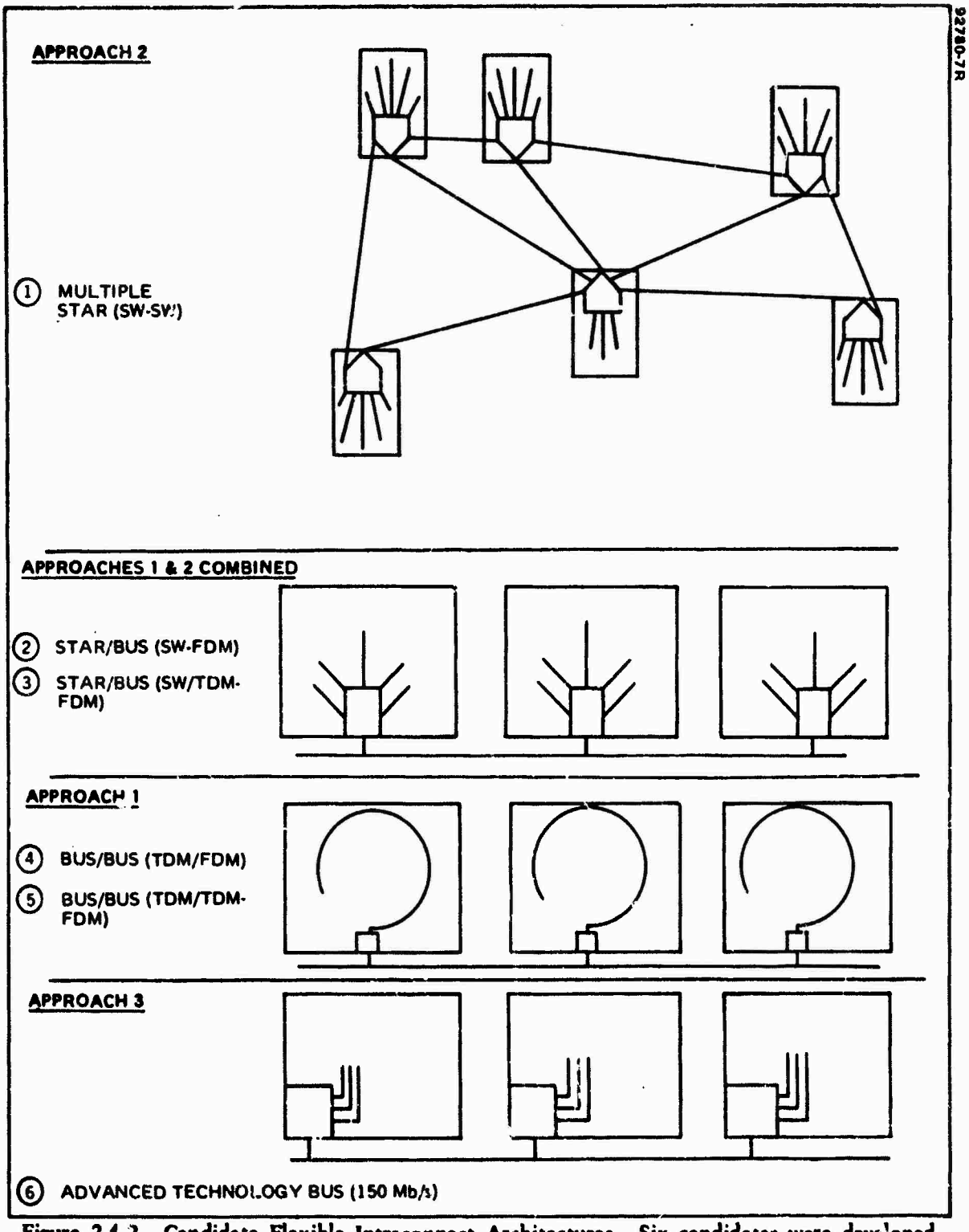

Figure 2.4-2. Candidate Flexible Intraconnect Architectures. Six candidates were developed from three basic approaches.

Part 2 – Summary of Task I, Conceptual Design Analysis

5. METHOD OF EVALUATION AND SELECTION

Selection of the most cost-effective FI concept was made via disciplined use of the weighted rating evaluation technique combined with cost, consistency, and sensitivity analyses.

Evaluation of FIs and selection of the most cost effective FI was a complex task. Six different FIs were evaluated with respect to a large number of criteria, considerations, and factors. The weighted rating evaluation technique was used to perform the evaluation of FIs and select the most cost effective FI.. The goals of the weighted rating trade-off approach were to 1) reach an objective decision in a logical manner and 2) to document and explain the evaluation and selection rationale.

There are several valid objections to the weighted rating approach. First, without discipline it is easy to make the numbers show anything desired. Thus, if the selection is known before the evaluation, the weighted rating only documents and explains the selection rationale or justification. Second, there is considerable difference in the manner in which different people convert subjective judgments into numbers. It is an imprecise process. However, it is no worse than placing subjective judgements into categories such as excellent, good, fair, and poor. Third, the method can involve sophisticated manipulation of fuzzy data. This includes making analyses of numerical data in which the uncertainties in the data exceed some of the differences in the processed results. The interpretation of the weighted rating evaluation results must be made with these objections in mind. However, no better method is known for reaching an objective decision and for documenting and explaining the selection rationale.

Figure 2.5-1 illustrates the main steps in the evaluation and selection approach. First the criteria and alternatives were defined. Then each criteria was given a weight indicating its relative importance in defining an overall figure of merit (FOM). Then each alternative was rated with respect ot its performance against each criteria. This rating was entered in the columns labeled R in the figure. Then the weight for each criterion was multiplied by rating of each alternative with respect to that criteria to provide the weighted rating (WR) points in the column labeled WR in the figure. These WR points were then added for each alternative to provide a sum which represented the figure of merit or measure of effectiveness (MOE). The difference between the FOM and MOE is the inclusion of cost in the sum of WR points for MOE.

A refinement to the weighted rating approach was the consistency analysis. This analysis examined the difference in WR points to determine whether or not they were consistent with the significance of the items. The differences in WR points were determined and were compared with each other. When logical inconsistencies existed, the weights or ratings (or both) were changed until the differences in WR points were more consistent with respect to each other.

The sensitivity analysis examined the extent to which ratings or weights has to be changed in order to change the order of the results. When such changes were reasonable, the conclusions were soft. When such changes were unreasonable, the conclusions were firm.

After several iterations of this disciplined evaluation technique by design team members, the Star/Bus FI concept was selected as the most cost-effective. It is described in the next topic.

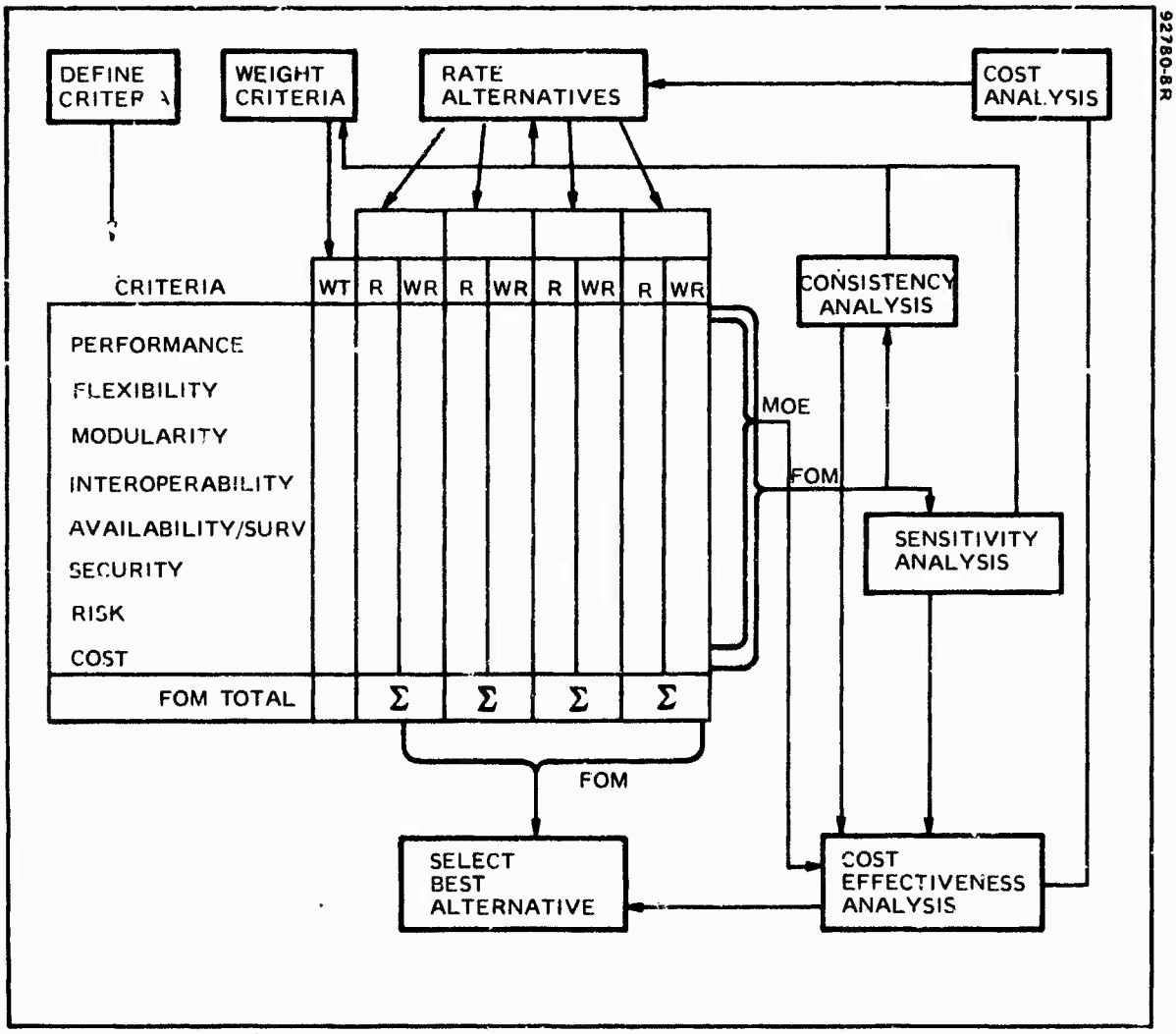

Figure 2.5-1. Evaluation and Selection Methodology. The weighted rating discipline was used to reach decisions logically and to document a traceable selection rationale.

Part 2 -- Summary of Task I, Conceptual Design Analysis

6. THE SELECTED STAR BUS CONCEPT

The selected FI concept is the Star/Bus Concept, a hierarchal approach which best meets the divergent requirements internal to, and between, shelters.

The selected FI concept is based on a TDMA microbus in each shelter which connects the equipments in the shelter with each other and with an FDM bus which connects all shelters of a center. The concept also provides for direct point-to-point connection between shelters where desired.

Although the quantity and types of equipments in C^3 centers for today and the future vary considerably, the topologies of all centers were found to fit a common patterr.. Equipments within shelters or facilities tend to be clustered in relatively close proximity to each other. Shelters and facilities, however may be colocated, or dispersed miles apart. For these and other reasons identified in the FI concept selection process a hierarchal Star/Bus topology (Figure 2.6-1, View a) was selected as the best FI Concept. Within shelters (facilities), a star topology permits few or many clustered devices to be connected star fashion to a TDMA microbus (a concentrated data bus device which evolved in Task III to be called the Local Intraconnect). The penalty in shelter weight is slight relative to a distributed bus, but the advantages in efficiency, control and cost of the concentrated TDMA microbus are great. Shelters or facilities with cluster of equipments are connected by an external distributed bus which ties all the TDMA microbus together. The external bus concept provides for coaxial cable implementation with the Time Division Multiple Access data carried in Frequency Divided Channels on carriers. *The External Bus concept lends itself to distributed control, high data capacity and low risk development for the near term. A second type of connection which permits direct point to point connection between shelters via coaxial or fiber optic cable is provided. This type of shelter connection offers a convenient option for intraconnecting centers consisting of a few shelters.

The TDMA microbus concept developed in Task I (see view b, Figure 2-7) takes advantage of the fact that all devices are connected to it in a star fashion with Device Interface Units (DIU, later called Local Intraconnect Units) buffering the data into a parallel time slot structured microbus. It was envisioned that each shelter could be fabricated with cables routed from DIUs to standard receptacles on the shelter walls, where devices with standard interfaces could "plug in". Alternatively, equipment cables could be routed directly to DIUs at the TDMA microbus. The microbus has the capability for implementing a very high capacity with very low risk. This is possible primarily because the bus occupies a very small volume. The parallel microbuses can be implemented on simple copper wire at a low cost, in terms of circuits and weight, because the bus services DIUs located only inches apart. 90 Mb/s capacity is achieved with circuits operating at 5 Mb/s, by using an eighteen-bit parallel microbus. Positive flow control is achieved with common

*In Task III, the fiber optic cable was adopted as the medium for the external bus.

timing and control circuits serving all DIUs and the Bus Interface Unit, (later called the External Intraconnect Unit). Propagation times for this bus implementation are negligibly short, resulting in efficient utilization of the data capacity. The Bus Interface Unit (BIU) provides the buffering and control interface between the TDMA microbus and the External Bus (later called the External Intraconnect).

The External Bus, implemented with coaxial cable, utilizes Frequency Division Multiplexing (FDM) to provide multiple carrier based channels. Some of these channels are allocated to wide band digital data in a TDMA bus and some can be allocated to other applications, such as radar data, conference video and high resolution imagery. The TDMA data bus implementation in the external bus is carried on three channels, each with a capacity of 20 Mb/s, resulting in a 60 Mb/s capacity external bus. The TDMA data bus buffered and controlled by BIUs completes the second hierarchal link, providing total connectivity between device equipments in shelters and between shelters.

Analog signals or other data handled in special external bus channels may bypass the shelter microbus and be presented to user devices directly by special device interface units.

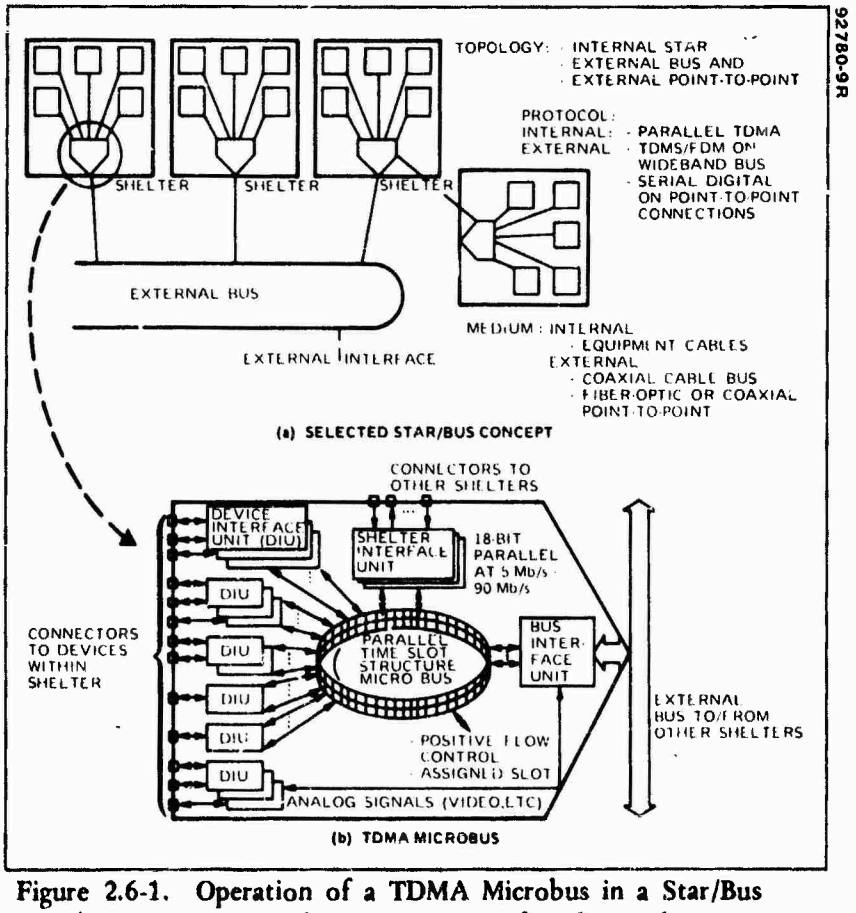

Figure 2.6-1. Operation of a TDMA Microbus in a Star/Bus Topology. A star topology is optimum for clustered equipments internal to each shelter. High capacity in a low risk, compact, economic unit characterizes the TDMA microbus.

PART 3
SUMMARY OF TASK II, INTERFACE ANALYSIS

Part 3 – Summary of Task II, Interface Analysis

1. REQUIREMENTS FOR INTERFACE ANALYSIS

Critical Interfaces within the flexible intraconnect were identified and analyzed in order to develop structures and protocol for positive flow control, high capacity and fast response.

The flexible intraconnect concept developed in Task I defined the most effective topology, protocol and media to achieve the Mod C^3 goals of modularity, connectivity, interoperability, flexibility and survivability. In Task II it was required to identify critical interfaces within that Flexible Intraconnect concept and analyze them to determine effective message structures, timing and protocol for achieving digital data transfer characteristics developed in Task I and further refined in Task II. Four critical interfaces were identified for analysis (Table 3.1-1). Critical interfaces include the interfaces with devices at the boundaries of the Flexible Intraconnect (Standard Interfaces and Accommodating Interfaces), and also the interfaces at the boundaries of the Local (Bus Interface) and External Intraconnects (Shelter Interface). In addition to the interface analysis, a Concept Verification Analysis was performed to verify that the FI concept, as it evolved in Task II still meet the requirements of TACS C^3 centers consistent with the TAFIIS Master Plan.

In Task II, analyses of the Local Intraconnect Interface (LII) (referred to as the Bus Interface in Government guidance) started with the basic structure developed in Task I (Figure 3.1-1). That is, a 90 Mb/s capacity implemented with 18 parallel 5 Mb/s Time Division Multiple Access buses, in a star connection. The analysis which remained to be done in Task II involved the development of a protocol and timing structure for the Local Intraconnect Interface which would meet message transfer and positive flow control requirements. In the analysis, message transfer requirements were further refined and developed to include Discrete Addressed and Broadcast messages and Virtual Bus channels. Messages could be as long as 1024 data words and there could be as many as 63 Virtual Buses. Up to 20 Mb/s capacity was allocated to Virtual Buses. The analysis resulted in development of a timing structure and a common control scheme, based on a reservation system of access to the Local Intraconnect.

A major requirement of the Task II Interface Analysis was to develop a standard interface—a point at which modular devices could be connected to the FI. The standard interface is one of the most critical features of the FI concept. With it, shelters can be produced with standard interface receptacles on the walls, such that modular devices with standard interfaces (computers, telephones, displays, etc.) may be "plugged in".

TABLE 3.1-1. SUBTASKS

The Task II effort consisted of analyses of the critical FI interfaces and concept verification.

- Bus (Local Intraconnect) Interface Analysis
- Standard (Preferred) Interface Analysis
- Accommodating (Selected Adapter) Interface Analysis
- Shelter (External Intraconnect) Interface Analysis
- Concept Verification

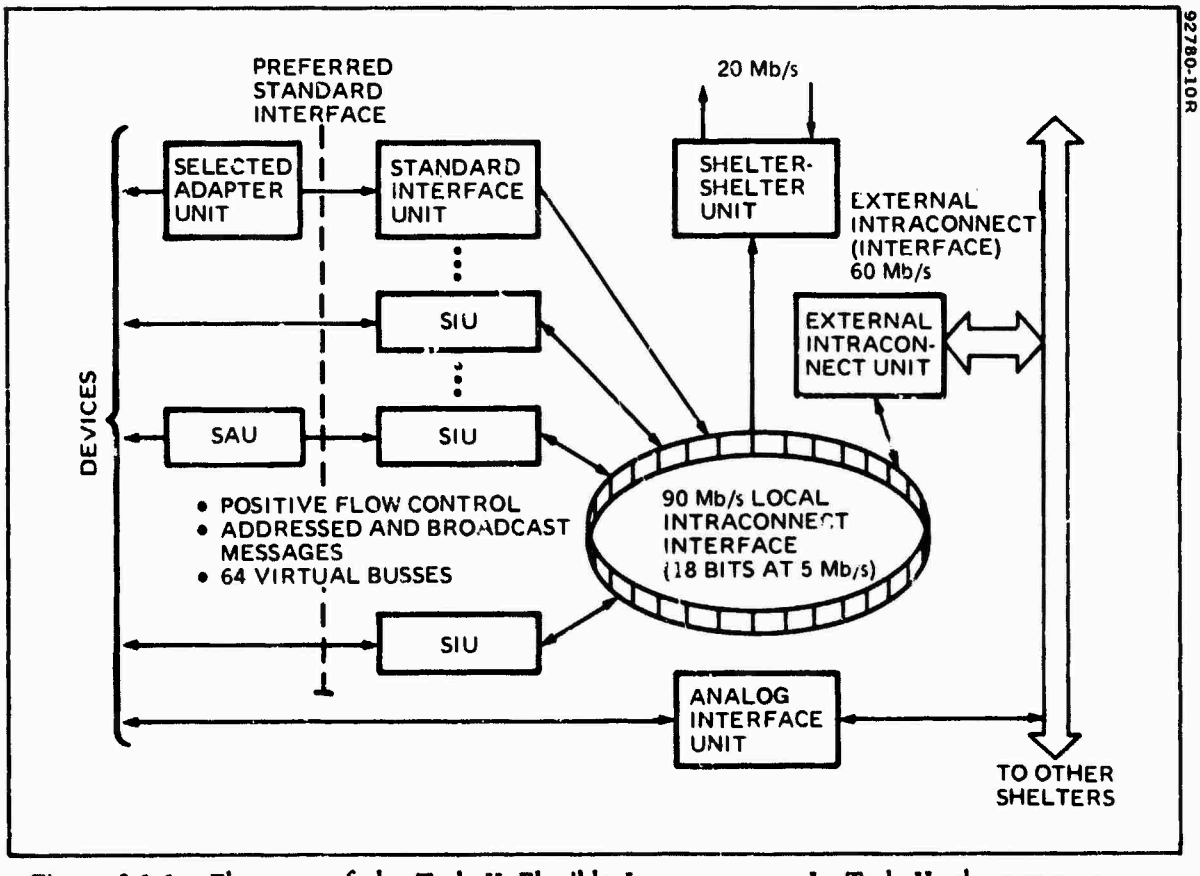

Figure 3.1-1. Elements of the Task II Flexible Intraconnect. In Task II, the structure, protocols, message formats and element names evolved, but the basic concept remained the same.

The Task II analysis initiated with the identification, analysis and development of the Preferred Standard Interface. With suggested examples of protocol, and desired characteristics as guidelines, potential candidates for the standard interface were developed and analyzed. The result of the analysis was a recommendation for a Preferred Standard Interface for the Flexible Intraconnect, documented in a Proposed Preliminary Military-STANDARD.

Although new C^3 devices could be developed with the Preferred Standard Interface, it was recognized that after the Flexible Intraconnect is introduced to C^3 centers many existing devices will not present standard interfaces. Also some new devices probably would be built without standard interfaces.

For these reasons accommodating interfaces were analyzed to determine the requirements for Selected Adapter Units to translate non-standard interfaces to the Preferred Standard Interface of the Flexible Intraconnect. A wide range of devices were considered in the accommodating interface analysis, resulting in a basic design approach for a family of Selected Adapter Units (SAU). It was determined that SAUs can be fairly simple microprocessor based devices, with plug-in modules to accommodate differences in non-standard interfaces. Also it was found that in many cases a single SAU type can accommodate a whole family of devices with similar interfaces (for example all devices with RS-232 interfaces). As a result of the analysis, top level SAU designs for a wide variety of suggested devices were developed.

The External Intraconnect Interface (EII) structure was developed in Task I with a TDMA bus and other channels implemented on a multichannel Frequency Division Multiplexed (FDM) coaxial cable. (Note: In Task III the EII evolved to a fiber optic cable). In Task II the timing structure, protocol of access, and control mechanism for supporting Block Message and Virtual Bus transfers on the TDMA bus were analyzed. FDM channelization options were also explored. The analysis resulted in the development of a protocol of access which is basically a reservation system, but which uses some dedicated and fixed time slots for efficiency, fast response, and distribution positive control, between shelters.

The Concept Verification Analysis utilized the techniques developed in Task I, to verify the FI concept as it evolved in Task II.

NOTE: In Task III the FI concept evolved to incorporate a Lazy Susan message system in addition to the Block message and Virtual Bus systems.

Part 3 – Summary of Task II, Interface Analysis

2. ANALYTICAL RESULTS FOR LOCAL AND EXTERNAL INTRACONNECT INTERFACES

A reservation system for access to the Flexible Intraconnect by interface units was found to be more flexible than assigned slot methods and less vulnerable than contention methods. Combining some dedicated slots with the reservation system enabled distributed control in the External Intraconnect.

Many techniques were evaluated for providing access to the FI. These were narrowed down to four methods which were examined in detail. Table 3.2-1 summarizes the advantages and disadvantages of the final four candidate time slot access methods. The tradeoff is based on data capacity, delay time, flexibility of access to time slots, operational dependability, hardware complexity and control requirements. Due to the different characteristics of the local and external intraconnects, slot access methods for these intraconnects were analyzed separately. The major differences for consideration of the Local and External Intraconnects are: (1) the Local Intraconnect, because of its physical and functional design can tolerate a central control approach; the external intraconnect cannot. (2) propogation times are significant in the External Intraconnect, not in the local. (3) External Intraconnects will usually have fewer shelters than Local Intraconnects have terminals. Common considerations are: (1) the need for operational stability (2) Time Division Multiple Access (TDMA) operation and (3) high throughput.

High Data rates (60-90 Mb/s), flexible message size (300-20,000 bits), short duty cycle (approximately one millisecond) and transfer characteristics (such as uniform or burst type) are of particular importance in determining the best design. For a network in which the subscribers transmit in a relatively uniform manner, the fixed assigned TDMA system generally provides for simple and effective data transfer. If the subscribers transmit at a low duty cycle in a burst mode, the contention scheme may provide efficient use of the available bandwidth of the communication network. However, contention schemes are generally limited to a maximum throughput which is much lower than net capacity in order to prevent the system from becoming unstable. For a network with a wide range of message types as encountered in TACS centers, a dynamic reservation system provides the most efficient use of time slots and presents no system stability problem.

Consistent with the above considerations, pure reservation and reservation combined with some assigned time slots, proved to be the optimum protocols for access to the local and External Intraconnects respectively. They apply to virtual bus, short and block message transfers. On the local intraconnect, prior to each message transfer, the desired number of Virtual Bus or standard time slots must be reserved. Reservations are made by reserving Virtual Bus slots during a fixed assigned slot segment of each Virtual Bus cycle. During each Virtual Bus slots can be reserved.

Short Block messages are transmitted on the external intraconnect using assigned slot portions of each cycle. Reservations for long Block transfers are made in fixed slots.

Characteristics of the local and external intraconnect interfaces, with the selected access protocol, are illustrated in Table 3.2-2. In this worst case example, providing 64 Virtual Buses totalling 20 Mb/s as well as an extensive Block message system, all operating with 8 shelters, the interface characteristics meet the FI design goals.

TABLE 3.2-1. TIME SLOT ACCESS METHOD TRADEOFF

Pure reservation and the combination of assigned slot and reservation access approaches are optimum for local and external intraconnect designs respectively.

METHOD	ADVANTAGES	DISADVANTAGES
Pure Reservation	• Flexible for block transfers • Flexible for short message transfers	• Complex Controls • Inefficient for short messages in EI • Requires Central Control
Assigned and Reservation	• Guaranteed Slots for each user • Provides block transfer flexibility • Simple transfer setup • No need of central control	• Must consider Propagation Delay for Assigned Slots • Not as Flexible as Pure Reservation
Contention	• Flexible • Short access time • Simple control	• Reduced capability due to collisions • Transfer rate must be limited to maintain stability • Overhead for acknowledgement • Risk of runaway
Fixed Assignment	• Simple timing structure • Simple control	• Inflexible for block transfers • Inefficient use of time slots

TABLE 3.2-2. LOCAL AND EXTERNAL INTRACONNECT INTERFACE CHARACTERISTICS. An example of how the access protocol and capacities are allocated at the interfaces.

	DIGITAL CAPACITY	TIME SLOT STRUCTURES	ACCESS METHOD	MAX ACCESS TIME
Local Intraconnect	90 Mb/s	---	---	---
Virtual Bus	20 Mb/s	Assigned Slot	Reservation	250 Microsec at 10 Mb/s
Block Messages	70 Mb/s	Fixed Slot	Reservation	250 Microsec
External Intraconnect	60 Mb/s	---	---	---
Virtual Bus	20 (16.6)* Mb/s	Assigned Slot	Reservation Slot	12 Millisec
Short Block Message	10 (3.2)* Mb/s	Fixed Slot	Assigned Slot	750 Microsec
Block Message	30 (28.3)* Mb/s	Fixed Slot	Reservation Slot	750 Microsec

*The bit rates of 20, 10, 30 are nominal; the numbers within the parentheses indicate the actual effective transfer rate.

Referring to Table 3.2-2, the terms "assigned" and "fixed" when used to identify slots are defined as follows:

- Assigned: For any given configuration, "assigned" slots are allocated to specific users.
- Fixed: For any given configuration, these slots are fixed with respect to the remainder of the timing structure but may be used by any device on a "first come - first served" basis.

3. ANALYSIS OF A PREFERRED STANDARD INTERFACE

Of the candidates that meet the modular requirements for a DMA transfer system, the 8080A protocol was selected as representing the lowest common denominator for the Preferred Standard Interface.

Preferred Standard Interface Candidates – Initial guidance in Task II directed the contractor to develop a standard interface for the Flexible Intraconnect and to prepare a preliminary Military Standard describing it. The interface protocol was to include one or two, but not more than three options selected from four suggested machine protocols. Of the four machine protocols suggested for consideration, three were defined by the Government and one was to be the contractor's choice. The government suggestions for protocol were the IBM 360/370 protocol, the Digital Equipment Corporation (DEC) PDP-11 protocol, and the Intel 8080A protocol. Hughes considered several military computers for its choice of candidates for the standard interface protocol but settled on the AN/UYK-40 mini-computer as the most competitive choice. Additional guidance regarding the standard interface oriented the selection towards a DMA block data transfer structure and protocol.

Selection of the Preferred Standard Interface – Of the candidate protocols considered, the DEC PDP-11 and Intel 8080A offered DMA transfer control protocol interface options that were most suitable for the FI standard interface. However, there was not adequate justification to select two protocols for the standard and therefore the simplest of the two, the Intel 8080A DMA transfer protocol was selected for the Preferred Standard Interface. The structure of the interface includes nine parallel (half word) data bits, transferred in a half duplex mode, controlled by four control lines (see Figure 3.3-1). The interface involves asynchronous control and can accept 8 or 9 bit-wide data structures. The half word (9-bit) structure is compatible with the 18-bit parallel data structure of the Local Intraconnect and offers compatibility with a wide range of peripheral and potential user devices. This preferred interface structure is expected to lead to the most cost effective mod C^3 systems because of its simple control protocol and half-word data structure. Future Mod C^3 devices can be readily built to present data in a preferred standard interface with this simple protocol. Full word parallel devices often have half-word optional interfaces; relatively simple SAU's are required when they do not. Serial data interfaces are also accommodated by relatively simple SAU's as described in subsequent topics.

Preferred Standard Interface (PSI) Operation – The PSI contains four asynchronous control lines: two for controlling data flow into the SIU and two for controlling data flow from the SIU. There are nine (9) bi-directional data lines to carry the data to and from the SIU.

The data transferred via the PSI occurs under positive control of transfer, in that a halfword is presented for transfer on the data lines when and only when the control signal from the receiving device indicates the input buffer of the receiver is not busy. When transfer occurs the receiver acknowledges acceptance of the data and then, and only then, is the data cleared from the sender's output buffer.

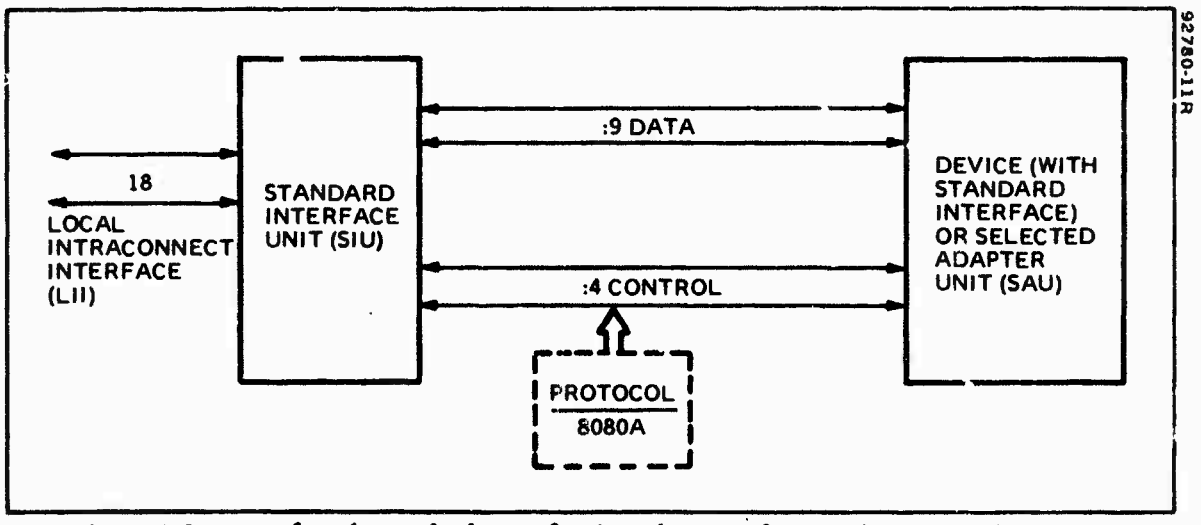

Figure 3.3-1. Preferred Standard Interface*. This interface is characterized by simple asynchronous control of 9-bit data transfers.

*Note: The Flexible Intraconnect design concept as it developed in Task III, maintained the four control line structure of the PSI, but expanded the data transfer to include full word (18 bit) transfer as well as half-word transfer. The logic of the control lines was further refined to include block as well as word transfer control.

4. PREFERRED STANDARD INTERFACE MESSAGE FORMATS

All messages include three basic sections, the header, the data, and the error check. Message control information is in the header.

The structure of standard messages as they are processed within the SIU is illustrated in Figure 3.4-1. Eighteen bit words are processed in the SIU, compatible with the structure of the Local Intraconnect Interface (LII). Data flows across the standard interface in nine* bit half words, but is converted to the eighteen bit word format in the SIU, * as illustrated in Figure 3-3. Each message is originally assembled by a device or its Selected Adapter Unit (SAU). This includes the required mode bits (virtual bus or block transfer), destination (broadcast or discrete address), source code, message length, data, end of message code, and error check word. This information is structured in the messages in the following ways.

Header Section – The header section contains bits to specify the mode, the destination of the data, the source of the data and in the case of a variable length block, the length of the data section in half words. The first word of the header contains mode and flag bits as well as the destination specified.

Data Section – The data section contains the information to be transferred. In variable length message blocks the data section is always terminated with an end-of-message (EOM) word that is considered to be part of the data section. The word count as specified in the header section and EOM code are tested to determine true end of message.

Error Check Section – The terminating word of each message block is an error check word. Error tests may be made at critical transition levels of the FI: Device (or SAU) to SIU, SIU to SIU via LII, SIU to EIU, EIU to EIU etc. When errors are detected status bits are set and appropriate logic responses initiated within the FI.

Message Types – There are two basic message types recognized and processed by the SIU: data messages and control/status messages. Data messages are variable in length, but control/status messages are fixed in length.

Data Messages – Three types of data messages are used to distribute data via the Flexible Intraconnect: discrete addressed data messages, broadcast data messages and virtual bus messages (Lazy Susan was added in Task III). All three types of messages are indicated in the header of the message structure. Since data messages are variable in length, a message length word is included to assist the SIU processing.

Control and Status Messages – Control and status messages are used within the FI for initialization, configuration control, assignment of SIU/device addresses, assignment of virtual busses, to test the FI, and to monitor status.

Data Flow Across the PSI – Message blocks are transferred in half-words across the PSI; internal to the SIU they are processed in full words. This full word to half-word conversion within the SIU is a simple but desirable transfer function which is expected to reduce the requirements for SAUs.

Figure 3.4-2 shows the movement of a data block from the LII, through the SIU to the associated device or SAU. The SIU receives the message composed of 18-bit words from the LIU under control of SIU selection gating. The message progresses through the buffer storage to the output control at the PSI. Each word is separated into half words and presented to the SIU output buffer.

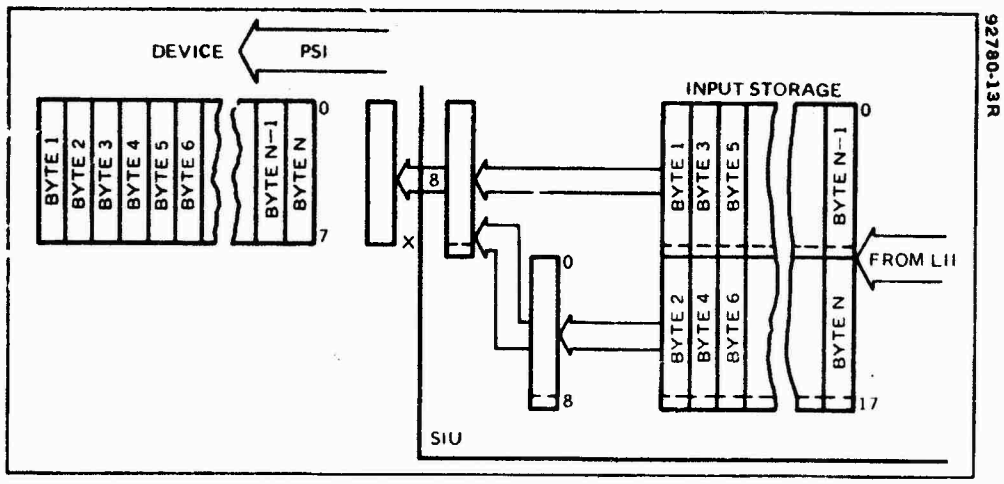

Figure 3.4-2. Data Flow – LII to SIU to Device. Byte oriented devices are accommodated directly by half-word transfer.

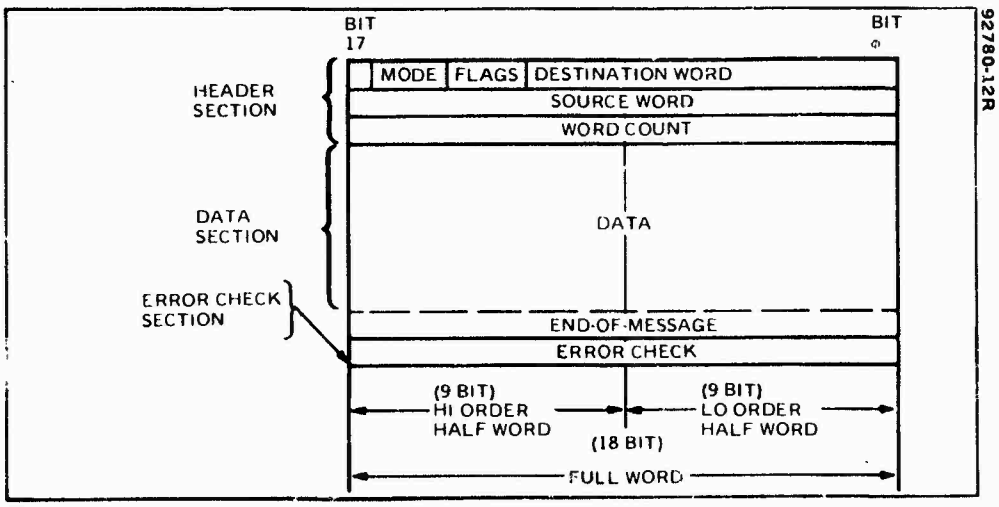

Figure 3.4-1. Structure of Message. A three-part message structure was established in Task II.

*Note: The Flexible Intraconnect Design concept as it developed in Task III, maintained the basic 3 part message structure developed in Task II, but expanded the Header to 16 words. The SIU became the LIU. Data flow across the PSI can be either 9-bit or 18-bit words.

5. SELECTED ADAPTER UNITS FOR NON-STANDARD INTERFACES

Microprocessor based Selected Adapter Units (SAU) accommodate a wide range of devices to the Preferred Standard Interface and provide a potential for plug-in convertability.

A preferred standard interface was developed such that future Mod C^3 devices could be developed with this interface and connect directly to the Standard Interface Unit of a Local Intraconnect. For those devices, both present and future, whose interface is different from the preferred standard, a Selected Adapter Unit (SAU) can convert the non-standard interface to the preferred standard.

A list of user devices and device categories (Table 3.5-1) were provided as guidance to the contractor to enable him to select representative examples for use in analyzing the requirements and design approaches of SAUs. One of the early conclusions drawn in the user device interface analysis is that many of the devices have common interfaces requiring common SAU designs. For example, many devices have NTDS Fast interfaces, all of which can use the same SAU designs. Similarly devices with RS-232 interfaces may use the same design SAU.

The configuration of the functional block diagrams for all SAUs is similar (Figure 3.5-1), with some functions common to all SAUs and some functions peculiar to each type of SAU. For example, the microprocessor control for all SAUs may be identical but the software algorithm determinant will vary between SAU types. Also the line driver/line receiver compliment on the device side will vary between SAU types. They are the same for all SAUs on the Preferred Standard Interface side. The conclusion from this analysis is that SAUs will be microprocessor oriented, with common types for many devices, and that SAU types may be convertable from one type to another via plug-in modules.

TABLE 3.5-1. USER DEVICES

A representative list of user devices provided as guidance for SAU analysis

360/370 COMPUTER AND PERIPHERALS
UYK-7
PDP-10
HAC LIQUID CRYSTAL DISPLAY
CCD MASS MEMORY
HP GRAPHIC PLOTTER
CRT TERMINAL
8080A PERIPHERALS
AND OTHERS

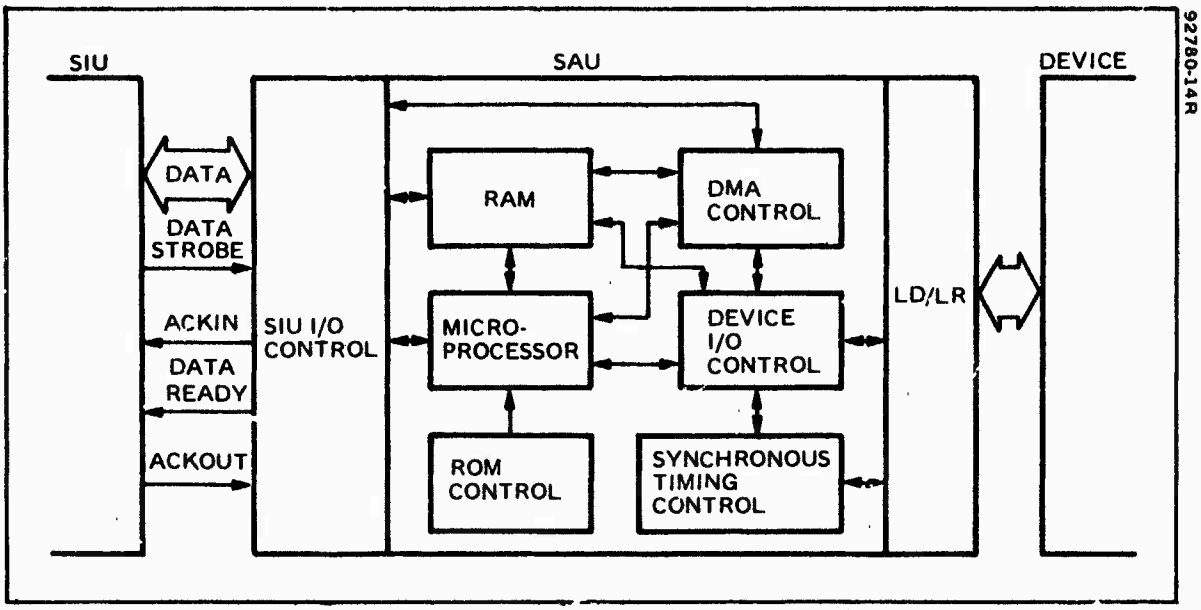

Figure 3.5-1. Device SAU Functions. The basic functional configuration of all SAUs is similar with some identical components and some device peculiar components.

Part 3 – Summary of the Task II, Interface Analysis

6. CONCEPT VERIFICATION ANALYSIS

The Flexible Intraconnect design concept, as it evolved in Task II, meets the flexibility requirements of the four System Configuration Concepts, derived from the revised TAFIIS Master Plan.

Four System Configuration Concepts (SCCs) were defined from the revised TAFIIS Master Plan in Task I to represent today's, tomorrow's, and future C^3 systems. The FI design concept developed in Task I was then verified for its flexibility to meet the changing requirements of the TACS by testing it against these SCC's. Since the SCCs were developed from the TAFIIS Master Plan they were again used as the test for flexibility of the FI concept as it evolved in Task II.

SCC-1 is essentially today's manual tactical air control system (TACS), with the exception of the CRC, CRP and ASRT which are automated centers. SCC-2 features an automated and upgraded TACS and SCC-3 integrates the intelligence functions in various centers while providing increased mobility. SCC-4 distributes the functions of CRCs among other centers which have self-propelled modules.

The initial approach in developing the SCCs was to define the present TACS as SCC-1. In order to evolve to SCC-2, Hughes reviewed the main operational functions of the TACS relative to command and control along with the present TACS organization. The near-term threat environment was also analyzed and a mission activity profile was selected based on data supplied by ESD/TAC for the SEEK FLEX program. The activity profile data were reviewed and augmented with estimates of hostile track data. The activity base was then extended for use in all TACS operational centers or facilities for SCC-2. Finally, major TACS development programs were reviewed to determine their impact on SCC-2. These near-term programs are detailed in Volume VII of the TAFIIS Master Plan and consist of such efforts as 485 L TACC automation, FACP automation, AWACS (E-3A), JTIDS and TRI-TAC. Based on all of the foregoing considerations, SCC-2 evolved based on changes to SCC-1.

Evolution of SCC-3 and SCC-4 proceeded essentially in the same manner. A set of guidelines was developed for synthesis of each SCC configuration based on the TAFIIS Master Plan as well as conceptual changes to the TACS and a revised top-level functional and information flow. For SSC-3 and 4, a determination of new operations that each center would perform was made, based on each respective center's operations as previously defined in SCCs 1 and 2.

Figure 3.6-1 illustrates the methodology used in both Tasks 1 and 2 for concept verification analysis. The effort in Task 2 is part of an iterative process which overlays the four SCCs on the design concept that has evolved for the FI. In the Task 2 verification analyses, the maximum operational loading for the busiest centers was reviewed for each SCC to determine if the FI

could satisfactorily handle it. For SCC-1 and SCC-2, the CRC was selected and for SCC-3 and SCC-4, the TACC (OPNS) presented the "worst-case" loading conditions.

The analysis verified that the evolved FI concept meets and indeed exceeds all anticipated maximum loading conditions.

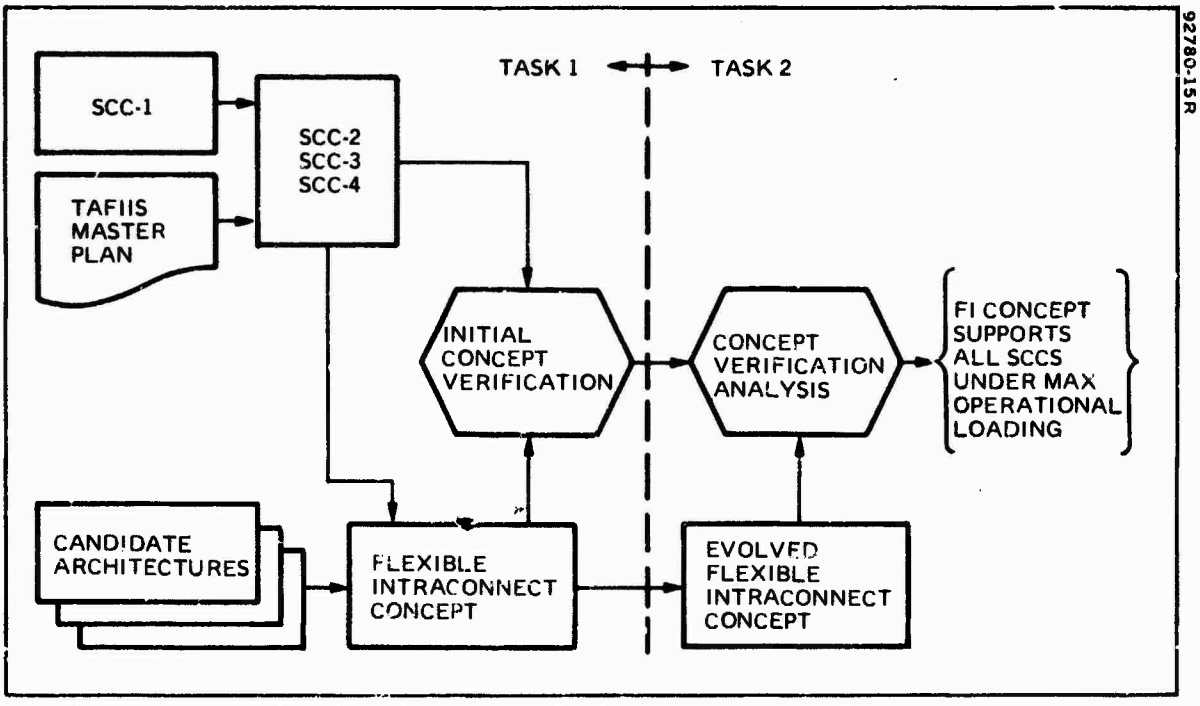

Figure 3.6-1. Methodology for Concept Verification Analysis. Four SCCs based on the revised TAFIIS master plan were used to verify the evolved FI concept.

PART 4
TASK III, PRELIMINARY DESIGN ANALYSIS

SECTION 1 – STATEMENT OF REQUIREMENTS

SECTION 2 – FI OVERVIEW

SECTION 3 – KEY ISSUES IN THE TASK III ANALYSIS

SECTION 4 – OPERATION OF THE LOCAL AND EXTERNAL INTRACONNECTS

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SECTION 1
STATEMENT OF REQUIREMENTS

Part 4 – Task III, Preliminary Design Analysis
Section 1 – Statement of Requirements

1. KEY MODULAR C^3 FI DESIGN CRITERIA

In addition to the Statement of Work, three basic design criteria were mutually agreed upon by the Government and Hughes for guiding the design of the Flexible Intraconnect: (1) positive control, (2) technology exploitation, and (3) provisions for capacity.

Early in the study the need became apparent for a set of design criteria, which were consistent with, but went beyond the Statement of Work and the TAFIIS Master Plan. Having identified a basic FI concept in Task I, and interface definitions in Task II, it was necessary to refine these concept and interface definitions in Task III, and to develop preliminary functional and implementation design data. There were many options of functional and implementation design that would satisfy the basic Mod C^3 requirements and would be consistent with the selected FI concept. For example, some design options emphasized implementation efficiency, but at the cost of positive control. Some optimized the design for near term implementation with less than optimum adaption to future developments. Other designs optimized the implementation with advanced and developing technologies where they offered significant advantages, and thus provided for alternate or interim implementations where technology advancement was not as rapid as projected. Although the need for agreed upon design criteria to resolve these issues came up in the Task II interface Analysis, it became paramount in the Task III Preliminary Design Analysis. At the In-Progress-Review (IPR) working sessions, the Government identified three primary criteria and their order of priority to be applied to the design of the FI. Definitions and applications of the criteria were refined and mutually agreed upon by Hughes and the Government. The criteria were then implemented and embodied in the preliminary design of the FI in Task III. The criteria are listed in order of priority and with amplifying examples in Table 4.1-1.

The first and most important criteria implemented in the design of the FI, is to provide for "positive control" of system operations. This criteria impacted the design in all aspects but primarily in the area of data transfer control. The choice of reservation control for FI access, with some assigned slots in a time slotted structure was directly influenced by this "positive control" criteria. While its implementation efficiency was desired, the control discipline of the reservation protocol won out over contention type protocols with their potential to lockup or runaway under heavy load. Predictable operation, under all load conditions, is critically important. In addition, "positive control" criteria drove the FI design to include front-end handshake as well as ACK/NACK control in moving messages through the FI, preventing the system from loading up with futile transmissions when a receiving node is "not ready". "Positive Control" of system operations also dictated that the FI design should provide for simple operator actions and operation. This was carried out in the FI design by providing for an effective FI Management scheme that permits automatic start-up and operation of the FI in a basic configuration with no operator interaction. In addition, a provision is made in the FI Management scheme for monitoring and

reconfiguring under software control, thus eliminating any need for sophisticated operator interaction, and potentially resulting in simple operator control.

The second priority design criteria is to "exploit the technology". This criteria caused the FI design to maximize digital implementation, and the control mechanisms to be designed to take advantage of microprocessor implementation. In Task I the FI concept was envisioned to be implemented with coaxial cable in the External Intraconnect, with potential evolution to fiber-optic cables. In Task III the design criteria to "exploit the technology" caused the design to reconsider, and optimize for fiber optic cable implementation, recognizing that coaxial cable could be implemented as an interim or fallback solution if necessary. Throughout the study, technology development has been continuously surveyed to exploit implementation in the FI where appropriate. Memory and surface acoustic wave (SAW) devices have received special attention.

"Capacity" is the third of the three most important FI design criteria. That is, the first two criteria are not to be sacrificed to achieve high capacity. Inherently, capacity is coupled with data transfer efficiency because information throughput is the ultimate measure of FI data capacity. The goal here

TABLE 4.1-1. FI DESIGN CRITERIA

- POSITIVE CONTROL
  - HIGHLY DISCIPLINED
  - NO LOCKUP
  - NO RUNAWAY
  - MINIMIZE UNPREDICTABLENESS
  - SIMPLE OPERATOR ACTIONS
  - AUTOMATIC CONTROL
  - RECONFIGURATION AND MONITORING IN SOFTWARE
- EXPLOIT THE TECHNOLOGY
  - MAXIMIZE DIGITAL IMPLEMENTATION
  - MICROPROCESSOR IMPLEMENTATION
  - FIBER OPTICS
  - MEMORIES
  - SURFACE ACOUTIC WAVE DEVICES
- CAPACITY (BUS EFFICIENCY)
  - ADEQUATE (SURPLUS) CAPACITY
  - INCREMENTAL DEVELOPMENT
  - INCREMENTAL IMPLEMENTATION

is to provide surplus capacity over what is estimated to be required by C^3 centers so that the system will not overload and control can be simple. It is also the goal, at this point, to design capacity into the concept so that growth can be accommodated incrementally, e.g., in the FI message structure data fields are allocated to accommodate up to 63 shelters, even though much less than that will be implemented initially. The full shelter complement may never be exploited but FI growth will not be limited by the concept. Also, the preliminary design developed in Task III is based on an implementation with 90 Mb/s in the local intraconnects and 60 Mb/s in the external intraconnect. These capacities are considered more than adequate for any TACS C^3 center and are used because they meet our capacity goals in an efficient, low-risk system. Inherent in the concept, however, is the ability to increase or decrease those capacities incrementally. For example, a system could be implemented with only 20 Mb/s capacity in the External Intraconnect, or it could be implemented with 100 Mb/s. Only the number of fiber-optic channels driven in parallel would change. Similarly the data capacity of the Local Intraconnects could be changed simply by changing the basic clock rate generated in the Local Intraconnect Control Unit.

SECTION 2
FI OVERVIEW

Part 4 – Task III, Preliminary Design Analysis
Section 2 – FI Overview

1. FEATURES OF THE FI DESIGN

The Flexible Intraconnect design provides connectivity for modular elements of C^3 facilities in a way that enhances the flexibility and interoperability of C^3 centers and elements. This design has applications to current systems as well as to systems that will be developed and operating in the 1990's.

Modularity and flexibility are important features of the FI design, but more important is the impact on Tactical Air Force C^3 Centers implemented with the FI. Center modularity and flexibility that result from the use of the FI enhances the operational capability and effectiveness of Tactical Air Control Systems. The interoperability of centers, and their improved survivability, potentially resulting fro FI implementation highlights the importance of the FI features listed in Table 4.2.1-1.

The FI is modular in the sense that is packaged modularly and it presents a standard interface to user devices, with device connectivity controlled by FI software. This FI modularity provides for C^3 center configuration flexibility in field operations, for center build-up, scale-down, and role changing, so necessary to support rolling force and leap-frogging tactics in future mobile environments. The modular FI design with standard interfaces for devices also supports incremental development of C^3 devices. For example, new C^3 devices can be developed with standard interfaces, and can be installed in centers without incurring the cost of modifying the centers or developing new centers. In addition, the FI packet or block message structure and the layered approach to interface protocols supports incremental development of C^3 software. The combination of incremental development and implementation of C^3 hardware and software capabilities provides for very economic upgrading of Tactical Air Control System capabilities. The economics resulting from reduced training, maintenance and logistics can be even more significant.

The FI Star/Bus approach, implemented with fiber optic connections between facilities or shelters provides for improved C^3 center survivability through wide geographical dispersement (up to 5 miles) of C^3 functions. Survivability is also enhanced by the ability to reconfigure the FI (hence the system), providing for continued, or degraded, operations in the face of C^3 functional losses. Functions, software modules, and data can be allocated to backup devices. Backup devices, and program modules can be brought on-line without interrupting operations. Reconfiguration services of the FI can even restructure the connectivity of the center and provide for program and data transfer necessary for degraded operations or for performing new functional roles.

Enhanced interoperability of centers can be expected by implementation of the FI. Standard interfaces and selected adapter units can accommodate all expected varieties of C^3 center external interfaces. Also the data capacity and layered protocol approach of FI data transfer systems can adapt to the wide range of information formats and control protocols of C^3 center external interfaces. Positive flow control in a highly disciplined, data moving FI protocol provides for the high degree of data transfer reliability and accuracy necessary for confidence in handling data from or to other centers.

The high capacity and data transfer modes designed into the FI not only meet current requirements, but accomodate evolving concepts for C^3 centers such as distributed processing, computer resource sharing, and distributed data base management.

TABLE 4.2.1-1. FEATURES OF THE FLEXIBLE INTRACONNECT

- Software control of the C^3 center connectivity
- Modular construction
- FI supports C^3 hardware and software modularity
- FI enhances C^3 center interoperability
- FI improves C^3 center survivability
- FI provides flexibility of C^3 center configuration
- FI accommodates distributed processing, data base and resource sharing

2. CHARACTERISTICS OF THE FI

The FI electronics, utilizing microprocessors for control, provide high capacity, connectivity, and versatility of application in a modular package occupying less than one third of a standard rack space in each shelter.

The Star/Bus heirarchal topology permits efficient implementation of the high capacity FI electronics in a small package. Typical shelter configurations, each with up to 20 Data Terminal Equipments (DTE) connecting to the FI, need only provide one-third of a standard 6 foot by 19 inch equipment rack in each shelter to house the FI electronics. This estimate uses preliminary design data based on implementation with circuits, modules, and cards from current military systems. The FI electronics in this estimate include 20 LIUs, 1 LICU, 1 EIU and FI power supplies, for each shelter. Other FI characteristics are listed in Table 4.2.2-1.

Whereas a typical large center would have no more than eight shelters total, with less than twenty devices per shelter, the FI control mechanisms and message structures are designed to accomodate up to 63 shelters and up to 63 devices per shelter, assuring adequate capacity for future growth or evolution. Operations analyses indicated that two miles is the maximum probable dispersion of shelters in a TACS C^3 center. However current fiber optic technology developments indicate that five miles is a reasonable performance expectation for field deployable fiber optic cables operated at 20 Mb/s per fiber. With three fibers being driven on the external intraconnect transmit bus and three on the receive bus, 60 Mb/s is achieved in the preliminary design. Higher capacities can be achieved by driving more fibers at that rate or by increasing the bit rate per fiber. For example a five fiber system would result in 100 MB/S in the external intraconnect. A rate of 90 Mb/s is achieved in the preliminary design of the local intraconnect with low risk by operating 19 parallel synchronous busses at 5 Mb/s. Other capacities in the LI can be achieved by changing the clock rate (up to 180 Mb/s). Changing the number of parallel busses would also alter the effective local intraconnect capacity but would have significant impact on the logic of the interface units.

FI information transfer systems are based on packets or message blocks with 16-word (18-bit) headers and variable data fields up to 1024 data words per message. Data throughput is clearly a function of average message length, since header length is fixed and data length is variable. However message/capacity utilization is in excess of 90 percent for all configurations, with message cycle times as short as one millisecond. Probably the most important characteristic of the FI, with respect to capacity, is its response to peak maximum load and capacity saturation conditions. Because of the highly disciplined reservation system of FI access, and positive control of information transfer, the FI will respond to saturation by operating at its maximum capacity. That is, it will be stable. It will not "run-away" with futile transfer attempts or control messages, as is possible in contention and non-handshake systems.

The data transmission systems implemented in the FI include 1) a Block message transfer system which transfers messages to discrete addresses or

broadcasts messages to all addresses on the FI, 2) a Virtual Bus transfer system with a maximum of 63 channels, and 3) a Lazy Susan system with a maximum of 63 simultaneous virtual rings. All systems operate within the Time Division Multiple Access (TDMA) structure of the FI, and are described in more detail in subsequent topics.

The FI concept is compatible with data encryption techniques. Interfaces for key-generation functions are identified in the preliminary design. Reliability estimates are based on preliminary design data and are discussed in more detail in subsequent topics.

TABLE 4.2.2-1. FLEXIBLE INTERFACE CHARACTERISTICS

CONNECTIVITY/CAPACITY
- Connectivity controlled by software
- Up to 63 LIUs for each local intraconnect (LI)
- Up to 63 LIs per EI
- DTE connections via standard interface
- Selected adapter units for non-standard interface devices
- Up to 5 miles between shelters
- Nominal bit rates: LI = 90 Mb/s; EI 60 Mb/s
- Maximum data rate per user device is 10M words/sec at 18 bits/word = 180 Mb/s
- FI response to capacity saturation: stable operation at maximum capacity
- Maximum message/capacity utilization: 90+ percent.

DATA TRANSMISSION
- Block message transfer: up to 1024 x 18 bit data words per message
  - Discrete addressed
  - Broadcast
- Up to 63 Virtual Buses
- Up to 63 Lazy Susan Networks
- Time division multiple access (TDMA)
- Access by reservation
- Reception available to all authorized subscribers
- Baseband modulation of digital data
- Distributed control among shelters
- Positive flow control via front-end handshake and ACK/NACK

ERROR RATES
- Less than one header error in 5,000 years
- Less than one undetected bit error in 10^{12} bits

RELIABILITY ESTIMATES (projected mid-1980's)
- LIU MTFB = 67,000 hours
- LICU MTBF = 93,000 hours
- EIU MTBF 88,000 hours

PHYSICAL (ESTIMATED)
- Size for a typical shelter: 1/3 of a 19 inch by 6 foot rack
- Power consumption for a typical shelter: less than one kilowatt, nominal

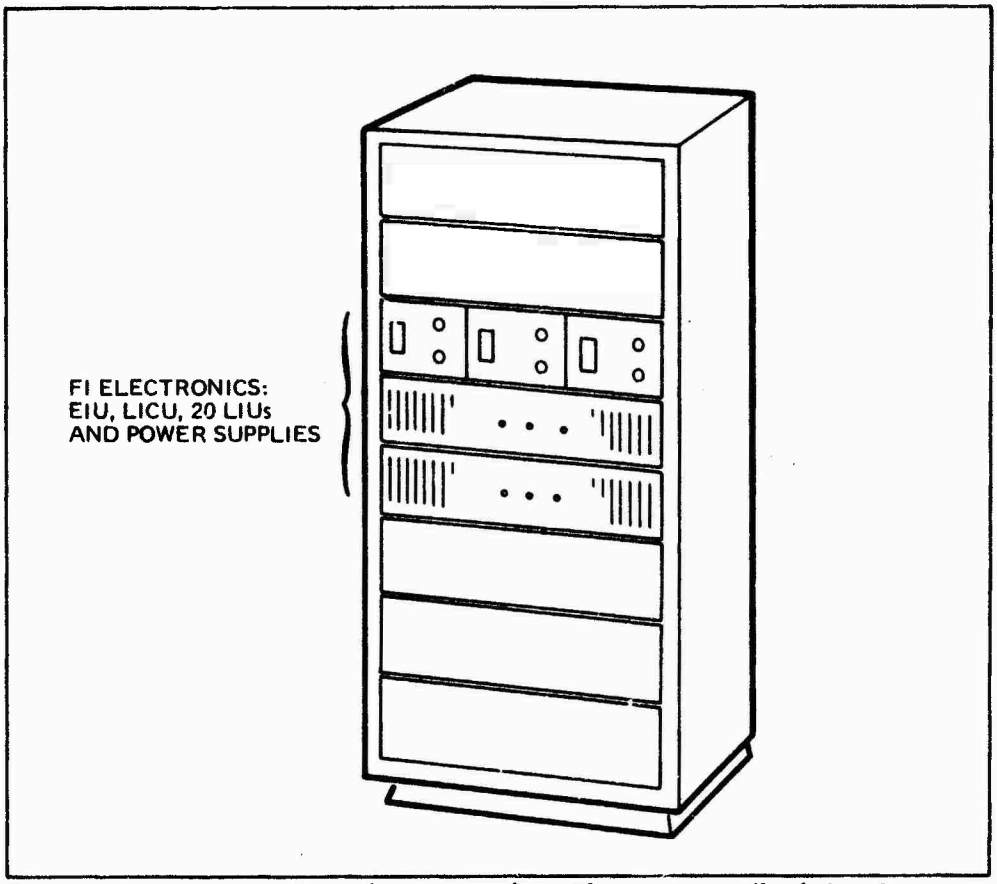


Figure 4.2.2-1. Physical Configuration of FI Electronics. All of the electronics required to support the FI in a typical shelter is indicated.

3. MESSAGE TRANSFER SYSTEMS

All information transferred within the FI is transported as digital data in message packets which are handled in three different ways within the FI, providing the flexibility to distribute information according to the needs of a wide variety of users.

Message Transfer Requirements – User devices (DTEs) and information systems in C^3 centers have wide ranging needs in terms of bit rates, quantities, and protocols of data transfer. Such needs will be even more pronounced in future centers than it is today, not because the roles and functions of tactical control are expected to change significantly, but because the systems performing these roles will be more automated, and more capable. They will be handling more data and will be performing more functions. In addition, future centers will implement distributed processing as well as data and computer resource sharing. Centers will have to handle the transient bulk data transfers associated with large data base and program module exchanges, as well as the steady information flow associated with "data base on the bus" operations. Low data rate users such as voice telephone (digitized), automatic data links, TTY and FAX will still be significant in C^3 operations. Also, there will be a need to handle short, irregularly occurring control messages with fast response time requirements. All these information exchange needs are served effectively and efficiently by the FI via its three message transfer systems: The Block message transfer system, the Virtual Bus (VB) system, and the Lazy Susan (LS) system (see Table 4.2.3-1).

Message Packets – The FI transfers all information (including Block VB, and LS data) in message packets in order to have the flexibility to simultaneously control a wide range of data quantity, rate, periodicity, and protocol. Each message is structured in a group of digital words, including a fixed message header and variable data field. The header contains information such as address and message type, needed to control the message transfer and direct it to its intended recipients. Transferring all data is message packets permits the FI to take advantage of high data capacity channels to service many lower data rate users, in virtual simultaniety, and to control the flow, rates, and access to the FI in a positive manner. The header content also permits the FI control mechanism to control messages in categorical message transfer protocols, such as the three message transfer systems listed in the table.

Block Message Transfer System – The Block message transfer system provides a control mechanism for transferring block of data from source devices to specific receiving devices via discretely addressed messages to all devices on the FI via broadcast messages. Block messages may vary in length from 32 up to 1040 eighteen bit words. Typical uses of the system include large data transfers such as memory dumps, program exchanges, total data base transfers, direct memory access retrieval, page display, and peripheral device data exchanges. Interactive messages such as command response

and other control messages also are optimally serviced by the Block message transfer system. Low data rate users such as digital voice traffic (16, 32, 64 Kb/s), digital data links (TADIL A, B, Link I, JTIDS), TTY, and facsimile are potential users of the block message transfer system.

Virtual Bus Transfer System – Within the Flexible Intraconnect, a control mechanism for regulating the use of the FI and for controlling the transfer of messages has incorporated which provides for reserving a portion of the FI capacity for a designated family of users. One of these guaranteed capacity information transfer systems within the FI is called a Virtual Bus (VB). The total set of VBs (up to 63) operating within the FI is referred to as the VB transfer system. A Sequence Number scheme for messages has been included in each message header and implemented in the FI control functions to provide for ordering user message transmissions within each of the VBs, so that device transmissions can be regulated according to data rate requirements of a family of user devices. As result, a family of user devices can be designated by one user, each member with its time ordered sequence and "metering rate" set up for its transmissions. The FI has the capability to allocate and control VBs according to requested requirements and to control the order of transmissions within each VB according to the Sequence Number assignments of each user in the family. The FI uses its FI Management function, Sequence Number, message type, authorization code and timing and control functions to perform VB setup and control. Sequence Number assignments to VB users may be performed by one of the users or by FI Management as a special service (See FI Management, Part 4, Section 10).

TABLE 4.2.3-1. THREE MESSAGE TRANSFER SYSTEMS

BLOCK MESSAGE TRANSFER SYSTEM

- Variable length messages up to 18 kilobits
- Discrete addressed messages
- Broadcast messages

VIRTUAL BUS

- Guaranteed/protected capacity within the FI
- Limited broadcast
- Metering rate control
- User managed
- 63 virtual buses, maximum

LAZY SUSAN

- "Virtual Ring"
- Time ordered sequential distributed processing
- User managed
- 63 Lazy Susan nets, maximum

3. MESSAGE TRANSFER SYSTEMS (Continued)

Although message transmissions are strictly controlled within each VB all user devices within a VB family will receive transmissions on that VB. The VB supports distributed processing, permitting implementation of the "data base on the bus" concept and computer resource sharing. Examples of C^3 functions for which the VB system is ideal are track data processing and distribution and display data distribution. Some voice and data nets will benefit from the guaranteed capacity and broadcast features of VBs.

Lazy Susan Transfer System – The LS system is operated within the FI TDMA network in manner very similar to the VB system, but to each user on a LS net it appears as though it is operating on a ring network. Thus, each LS is a "virtual" ring. It is a controlled access network, but its sequence number scheme is used to circulate messages around a ring of users in a time ordered manner. Each user in a ring listens only to messages transmitted by one other user in the ring. The user may or may not modify each message it receives before it passes it on. The virtual ring is organized so that messages circulate to all members, like plates on a "lazy susan". The originator of each message has the responsibility to remove its message from the LS ring after one complete cycle. Like the VB, each LS net may be managed by one of its users or by the FI Management function as a special service. There may be up to 63 LS nets designated and controlled within the FI at any one time. The LS nets will be used where sequential time ordered distributed processing is important, and where processes rather than addresses are critical. Suggested applications include track message updating, intelligence data processing and sharing, and Frag Order processing the LS have been considered for distributed processing and for distributed data bases.

SECTION 3
KEY ISSUES IN THE TASK III ANALYSIS

Part 4 – Task III – Preliminary Design Analysis
Section 3 – Key Issues in the Task III Analysis

1. IDENTIFICATION OF ISSUES

As a result of technology developments and factors encountered in preliminary design tasks, nine issues emerged as dominant considerations for Task III analyses.

Preliminary design issues in Task III caused the analysis to focus on FI implementation considerations with emphasis on FI capacities, control mechanisms, message structures, and transfer media. In addition, interfaces analyzed in Task II were further refined in Task III. New issues, addressed in detail, included specific implementation for positive flow control, development of an FI Management scheme, top level functional design of FI units, an error analysis, and a reliability analysis. Nine issues which received major attention in Task III are listed in Table 4.3.1-1.

Since the conceptual design studies in Task I were completed, fiber optics, microprocessor, and memory technology developments have advanced at unprecedented rates. Microprocessor and memory developments continue to support the FI design concept developed in Task I. Fiber optics technology developments, on the other hand, have advanced to the point where, in Task III, it was decided to reconsider the media issue in the External Intraconnect. The Task I conclusion was that the preferred approach for the External Intraconnect was to optimize the design for coax cable implementation, with the opportunity to convert to fiber optic cable implementation when technology developments supported it.

In Task III it was concluded that the External Intraconnect design should be optimized for fiber optics with provisions to fall back on a coax cable implementation if necessary in the future. Because of the differences in characteristics of fiber optic cables as compared to coax, External Intraconnect topology and protocol issues had to be re-analyzed. The considerations that led to selecting a transmit bus/receive bus topology with reservation access protocol are discussed in the next topic.

Refinement of the Preferred Standard Interface continued to be a major issue in Task III, involving increasing the PSI data transfer format from nine bit parallel to eighteen bit parallel (with a 9-bit operational option), refining the control line protocol, and expanding the definition of message structure content.

Layered protocol approaches being implemented in other national and international data transfer standard developments were analyzed; this resulted in an impact on the Preferred Standard Interface definition. For example, the block message structure and header content were designed to permit Device Terminal Equipments to use the FI as a data transfer medium but to operate with their own higher level protocol requirements. In addition Virtual Bus and Lazy Susan control mechanisms were designed to allow users to set up their own Virtual Bus or Lazy Susan networks and to manage them according to their own needs with higher level protocols.

TABLE 4.3.1-1. KEY ISSUES IN TASK III

- External Intraconnect Redesign
  Media, Protocol and Topology
- System Capacities/Capabilities
  Conceptual vs Implementation
- Preferred Standard Interface
  Design, Definitions and MIL-STD-XXXX
- External Interfaces
  Selected Adapter Units and Higher Level Protocols
- Positive Flow Control
  Bottlenecks & Saturation Prevention
- FI Management
  Management Service vs Critical Control
- Implementation
  Central vs Distributed Processor vs Special Purpose Logic
- Error Analysis
- Reliability Analysis

1. IDENTIFICATION OF ISSUES (Continued)

Table 4.3.1-2 illustrates an interpretation of a seven layer protocol definition as it applies to the Flexible Intraconnect and the Preferred Standard Interface.

Preliminary design of the FI involved analysing the distribution of functions in the FI and settling on implementations that exploited the technology without incurring inordinate development and operational risks. Although the same issues of distributed and central control had been settled in Task I, it remained in Task III to determine the manner of implementing those control functions. An external intraconnect design that efficiently incorporates distributed reservation control and positive flow control into the timing structure results from these analyses and is described in the Timing Structure section of this report. The balance between distributed and central local intraconnect control functions also resulted from these analysis. For example Local Intraconnect reservation control is implemented in each shelter by the Local Intraconnect Control Unit, a much more economic approach than distributing redundant control functions to all LIUs. Most of the control functions in the FI units may be performed by microprocessors but program step and timing analysis made it clear that input/output gating on the Local Intraconnect, External Intraconnect, and Preferred Standard Interface should be performed by special purpose logic because of the speed requirements. Decreasing memory costs and increasing memory sizes, available on chips, encouraged larger buffers and increased memory utilization; but the increased use was constrained by reliability and error rate considerations.

Task I analyses developed minimum FI data rate and connectivity capacity requirements; Task III analyses determined that increased capacities should be designed into the FI where the technological considerations supported it in order to provide for future growth and expansion of the concept. For example, the capability for 63 shelters and 63 devices is designed into the message structures and control mechanisms of the FI even though lower numbers were required by Task I operations analyses. Fiber optic implementation of the External Intraconnect will permit displacements of as much as 5 miles between each shelter even though 2 miles maximum dispersion of shelters was indicated by Task I deployment studies. Low risk technology permits 60 and 90 Mb/s implementation in the FI even though 27 Mb/s was the maximum load analyzed in Task I.

External C^3 center interfaces were examined again in Task III to determine the requirements on FI preliminary design and the resulting effects on center interoperability. The conclusions were that the FI supports and enhances the interoperability of centers via their standard interfaces, selected adapter units, high capacity, and flexible layered protocol approach.

FI Management requirements and design approaches were analyzed in Task III; this resulted in an approach which is based on automatic control implemented as an on-line FI function, with management services (such as reconfiguration and monitoring), implemented off-line as a service function.

Error analyses performed in Task III determined (and verified) adequate header and data error processing mechanisms, and identified critical error contributors in the FI. A major impact of the error analysis was on the total flow control processing method. Total ACK/NACK control was implemented throughout the FI, from LIU to LIU, to negate the potential introduction of errors by buffer memories, as well as long cable runs.

Reliability analyses were performed, based on preliminary design of FI units. The predicted reliability for FI units and typical FI configuration is very encouraging. However the sensitivity of failure rates to memory content encouraged constraint in the tendency to increase control buffer sizes. Reliability analyses are reported in detail in section 4.11 of this report.

TABLE 4.3.1-2. LAYERED PROTOCOL APPROACH

RESPONSIBLE	LEVEL	NAME	EXAMPLES
FLEXIBLE INTRA CONNECT (FI)	1	Physical Layer	PSI Physical Structure, Block & Word Transfer Control
	2	Link Layer	Block & Header Protocol, Error Codes and Control
	3	Network Layer	Virtual/Real Address, Handshake
DATA TERMINAL EQUIP (DTE) USER	4	Transport Layer	VB and LS Operation, Data Nets, Console Nets
	5	Session Layer	Computer-Console, Phone Hookup, Directed Data Stream
	6	Presentation Layer	Data Strip, Format & Decode
	7	Application Level	Higher Level Language-Fortran, Algol, Display

2. EXTERNAL INTRACONNECT REDESIGN

Fiber optic cable and supporting component technology has developed at such an accelerated rate since Task I that it was decided to redesign the External Intraconnect with optical fibers as the primary transmission media.

In the Task I conceptual design analysis, the selected FI concept was based on a coaxial cable implementation of the External Intraconnect. At the time, fiber optic cable was not selected as the primary media in the baseline design because it was judged to be too risky for 1979 implementation.

Since that time fiber optic technology has progressed more rapidly than expected and fiber optic links capable of operating at 20 Mb/s over 8 kilometers have been delivered to the US Army for field deployment testing. The MITRE Corporation has successfully demonstrated the use of fiber optic links for multiplexed phone and data applications in operating U.S.A.F. C^3 centers. The ITT Corporation and others have developed single fiber optical waveguides that exceed Mod C^3 requirements at projected reasonable costs. Adequate optical transmitters and receivers are currently available. The Hughes Aircraft Company is developing optical couplers, splitters, and fiber optic cable connectors that reduce the cost and development risks associated with field deployment of fiber optic cable data busses. All the problems associated with fiber optics application to field deployable tactical C^3 systems have not yet been solved; but fiber optic technology progress has accelerated to the point where, in Task III, implementation of the External Intraconnect with fiber optic cable was reconsidered (see Table 4.3.2-1).

Reconsideration and preliminary design analyses led to the conclusion that the External Intraconnect will be implemented with point-to-point fiber optic links between the shelters, with electro-optical regeneration (repeating) at each shelter (in the EIU). A low-risk design approach utilizes 20 Mb/s on each optical fiber, requiring three fibers for 60 Mb/s capacity, but accommodating up to 5 miles cable run between shelters. As shown in Figure 4.3.2-1, provision is made in the design to implement a passive bypass around each shelter which permits continued, uninterrupted operation of the Flexible Intraconnect in the event of a shelter loss. The EI operates with a transmit bus and a receive bus topology, permitting propagation time compensation by the harmonization of transmission times at each shelter. (A desirable benefit of the selected EI implementation is that it has the flexibility to be configured in a star topology as well as a bus topology.) The protocol of operation selected for the EI is a time slot structured (time division multiple access (TDMA) network) with some slots accessed by reservation and some slots assigned. As analyzed in Task II, this combination bus access protocol provides a maximum of flexibility with highly disciplined stable control.

Power budget analyses indicated that all-passive coupling of the fiber optic EI would be too limiting in terms of maximum quantity of shelters, and their maximum dispersement. Passive fiber optic coupling also limits configuration flexibility. However, point-to-point links with active regeneration

TABLE 4.3.2.-1. CHARACTERISTICS OF A FIBER OPTIC CABLE EXTERNAL INTRACONNECT

MEDIA:

- Fiber Optic Cable: 3 fibers at 20 Mb/s each
- Electro-Optical Regeneration at Each Shelter
- Passive Bypass at Each Shelter

PROTOCOL:

- Slotted TDMA Structure
- Reservation and Assigned Slot Control

TOPOLOGY:

- Transmit Bus/Receive Bus with Propogation Time Compensation

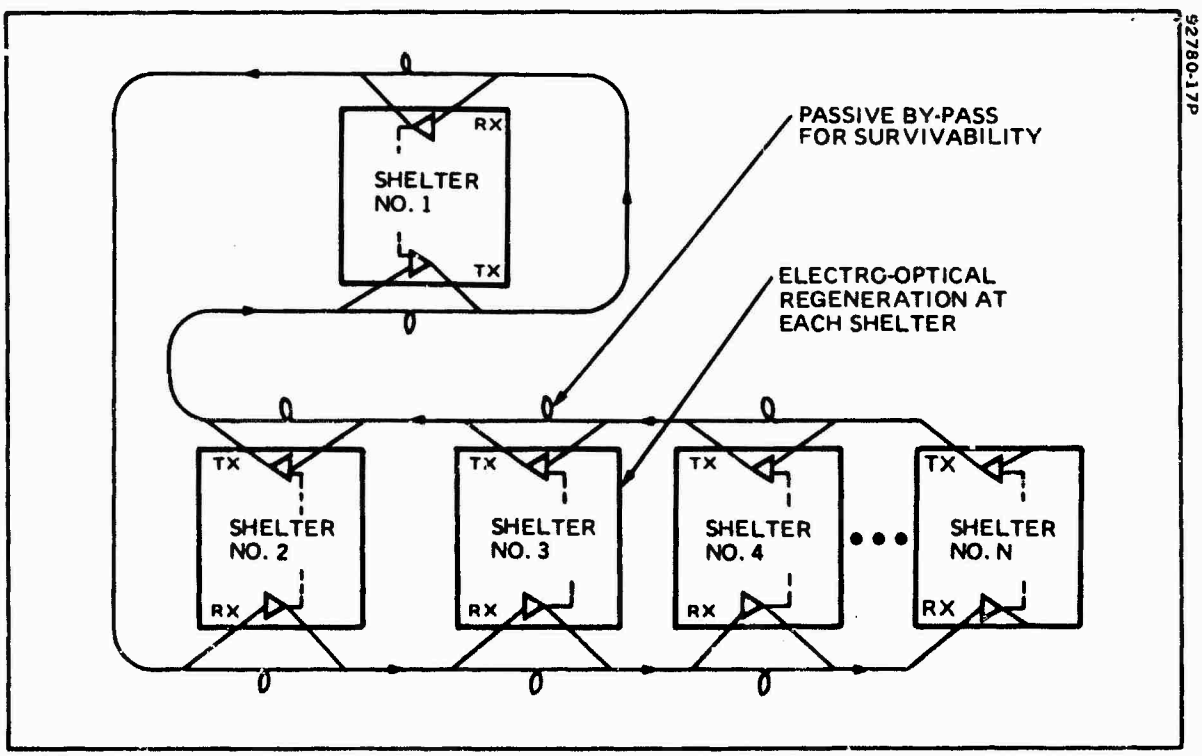


Figure 4.3.2-1. TX/RX Bus Topology on Fiber Optic Cables. It provides propogation time compensation without wasteful guard times and permits reconfig uration to a star topology when desired.

2. EXTERNAL INTRACONNECT REDESIGN (Continued)

at each shelter, overcome all of those limitations and in addition permits operation of an almost unlimited number of shelters, with up to 5 miles between shelters. (The Task I coax concept was limited to less than 8 shelters with a total dispersion of 2 miles.) Because fiber optic waveguides are practically limited to unidirectional operation, no additional cabling is required for operating a transmit bus and a receive bus than for a bi-directional bus. Message transfer efficiency analyses showed that the fiber optic transmit/receive bus is 90% efficient for all combinations up to 63 shelters. (The Task I bi-directional coax implementation message transfer efficiency was acceptable only up to 8 shelters.) Preliminary design analyses showed that it is possible to operate a fiber optic link with frequency division multiplexing (FDM); however technology has not advanced far enough to support FDM operation on fiber-optic cable as a low risk field deployment approach. Therefore space division multiplexing, channelizing by individual fibers, was selected for the EI; 60 Mb/s capacity is achieved by three fibers operating at 20 Mb/s on each bus (20 Mb/s represents a low-risk approach for the associated electronics). Additional channels can be provided by adding additional fibers and associated electronics.

In addition to the characteristics discussed previously, the decision to design the External Intraconnect with fiber optics was influenced by the potential for growth and additional capability offered by this rapidly developing technology. Because of the low weight of optical fibers, faster and easier de deployment of C^3 centers can result. (Hughes is currently developing rapid payout fiber optic systems that may have potential for C^3 center deployment applications.) Fiber optic waveguides offer bandwidth potential which far exceeds that being implemented in the current design. Longer ranges, hence more flexible configuration applications, are likely to result from fiber optic developments. In addition, fiber optic cables offer more security than electromagnetic media.

It is recognized that fiber optics still offers some developmental risks for application in field deployable military systems. Environmental considerations, such as dirt, temperature, moisture, and rough handling have not yet been totally accounted for in fiber optic component developments (although current projections are encouraging). In the event that these developments do not progress at the required rate, the External Intraconnect can be implemented with coax cable. This "fallback" design approach requires modifying only the transmitter and receiver functions of the EIU.

SECTION 4
OPERATION OF THE
LOCAL AND EXTERNAL INTRACONNECTS

1. FI TIMING STRUCTURE CONSIDERATIONS

A time slotted structure, with some slots available by reservation, and some fixed-assigned, provide highly efficient and stable TDMA busses in both the local and External Intraconnects.

Timing structure, access methods, message transfer protocol communication ranges, and vulnerability to failure were major concerns in the design of the FI. The techniques used had to be capable of handling the required data rate efficiently, to offer simple control protocol providing rapid access and allow the use of available hardware. During the FI design, many techniques were evaluated against the specific requirements imposed by FI operation: the trade-offs were based on positive control, data capacity, network efficiency, propagation delay considerations, flexibility of accessing network timing, and operational simplicity, and hardware complexity. Since the FI is constructed with Local and External Intraconnects, each with different characteristics, the techniques selected had to provide satisfactory solutions to the common and unique problems of both intraconnects.

A TDMA system was devised as the basic FI timing structure. The access methods and the message transfer control protocol were developed and tailored to the requirements and characteristics of each intraconnect. The purpose of the design was to offer the high efficiency, simple operation and implementations which are generally imbedded in the TDMA system. For a network in which the subscribers transmit in a relatively uniform manner, the fixed assigned TDMA slots generally provide simple and effective data transfers. For low duty cycle, burst type transmissions, a contention scheme provides efficient low cost use of the available bandwidth, however, at the risk of becoming unstable. To provide for uniform transmission needs and control functions as well as burst transmissions both, assigned slot and reservation schemes were selected for FI time slot access.

The FI design accommodates Virtual Bus (VB), Lazy Susan (LS), and Block message transfers, as depicted in the figure. The Local Intraconnect services the Local Intraconnect Units (LIU), Local Intraconnect Control Unit (LICU) and the External Intraconnect Unit (EIU). The external intraconnect services the EIUs in each shelter. Messages can be transferred locally via the LI between LIUs in the same shelter or externally via the LI and the EI to LIUs in other shelters.

During local transmission, assigned slots are provided for VB or LS messages. VB or LS message transfers take place when the appropriate VB or LS time occurs since the participants of a VB or LS transmit in accordance with preassigned sequence numbers. The VB message is broadcast to all users in the FI but LS messages are received in a sequential order according to the sequence numbers. VB or LS messages generated by an LIU are transmitted locally as well as externally via the EIU and EI to the LIU's of other shelters.

Prior to each Block message transfer, the LIU must make reservations with the LICU indicating destination address and message length. The LICU controls transmission via a transfer enable line and the data bus. Transmission handshakes are accomplished via (1) memory status messages which each LIU periodically reports to the LICU, and (2) ACK/NACK replies at the end of each message transfer.

The External Intraconnect interface consists of a transmit bus and a receive bus, each with three parallel fiber optic links transferring data at a rate of 20 Mb/s. A cycle is defined for the external timing structure (each cycle lasts for 1250 time units TU)). In each cycle, assigned slots are provided for VB or LS message transfers and a slot is also assigned to each EIU for short Block message transfers. For each Block message transfer, a front-end handshake and an ACK/NACK of message transfer status occurs. This handshake procedure is accomplished via assigned handshake slots.

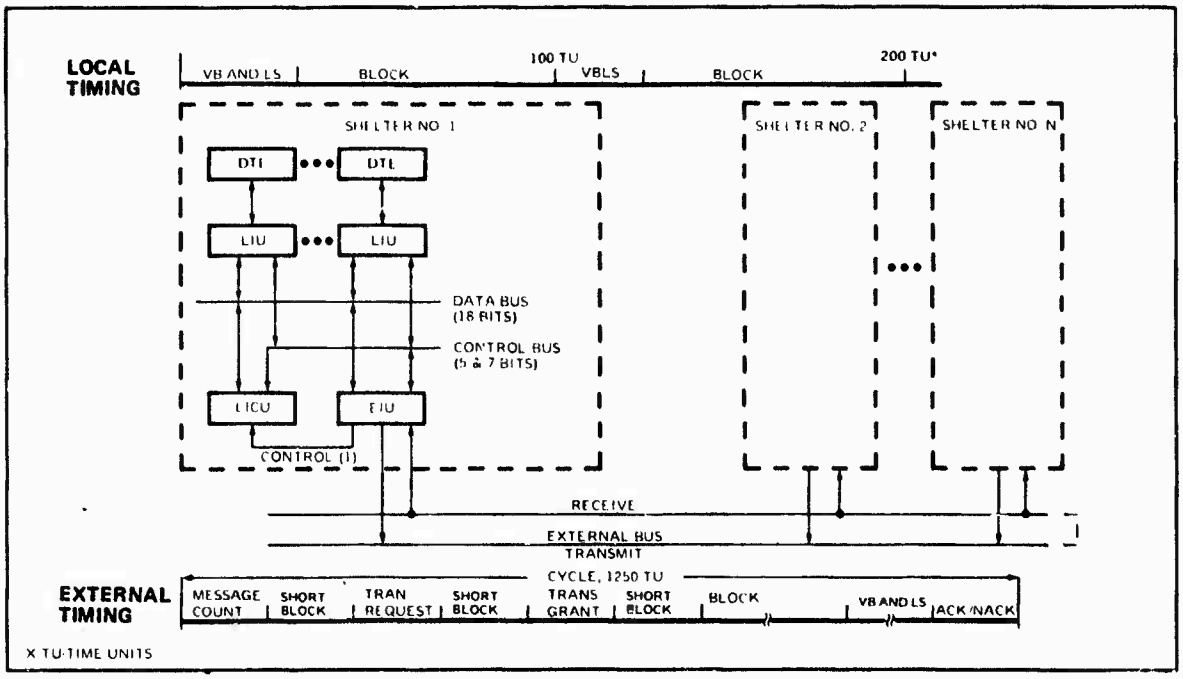


Figure 4.4.1-1. Overall FI Structure. Separate timing structures for the Local and External Intraconnects optimizes the use of reservation and assigned slots.

2. LOCAL TIMING STRUCTURE

Efficient message transfer on the Local Intraconnect with positive flow control is achieved via complementary data and control bus timing structures.

Various types of Data Terminal Equipments (DTE) are installed in a shelter to perform C^3 functions. Transfer timing, message routing, data capacity, and traffic handling are important factors to be considered in developing an efficient, flexible, and positively controlled Local Intraconnect. A network with short transfer delay is required and bottleneck and network staturation problems must be prevented. The timing structure must fit various message characteristics and minimize redundant retransmissions.

The short distances (inches) between the LIUs, LICU and EIU on the Local Intraconnect, together with efficient flow control make possible the use of a moderate speed data bus and separate control busses. The LIUs and the EIU transfer messages on the Local Intraconnect data bus in accordance with timing and control signals transmitted via a control bus and the data bus. The data bus is a uniformly time slotted 18-bit parallel network with time slots apportioned to block message, Virtual Bus and Lazy Susan transfers. The control bus provides reservation and transmission control for Block message transmissions, LIU status reporting, and VB/LS timing. (See Topic 4.6.A.3 for a description of the control bus interface.)

The overall timing structure is shown in Figure 4.4.2-1. The use of a programmable time unit instead of absolute time allows design flexibility for different operational needs. (A typical Time Unit (TU) can be one microsecond.) The selection of the same value of time unit for all shelters simplifies timing design and FI Manager timing configurations. In an operational environment where high bus capacity with short message lengths is required, a short cycle time is desirable. For low bus capacity and long message lengths, a long cycle time can be used. In either case, the cycle time length is programmable and is configurable by the FI Manager.

The Block (B) transfer time is shared by all the LIUs, the LICU and the EIU in any one shelter. Reservations are made prior to each Block message transfer by the use of a reservation request containing the destination address and the message length. Since the VB, LS and Block transfers use the same 18-bit data interface, possible transfer conflict is avoided by temporarily interrupting Block transfers during the VB or LS time slots. The reservation control provides each LIU a time for Block transfer reservations. The reservation consists of a 3 word interchange between the LICU and each LIU. The first word is placed on the bus by the LICU. It contains the address of the LIU that is being polled for reservation requests. LIUs are notified of the polling action by activation of the "reservation enable" line. The second and the third words, indicating destination addaddress and message length, are transmitted from the LIU to the LICU.

When enabling a Block message transfer, the transmission enable line is activated and the first word is transmitted from the LICU to poll the transmitting LIU. At the end of each message transfer, time slots are provided for

ACK/NACK transmitted by the receiving LIU. The ACK/NACK is transmitted in the last word of each transmission enable period.

The Local Intraconnect timing design provides a greater than 90% message transfer efficiency.

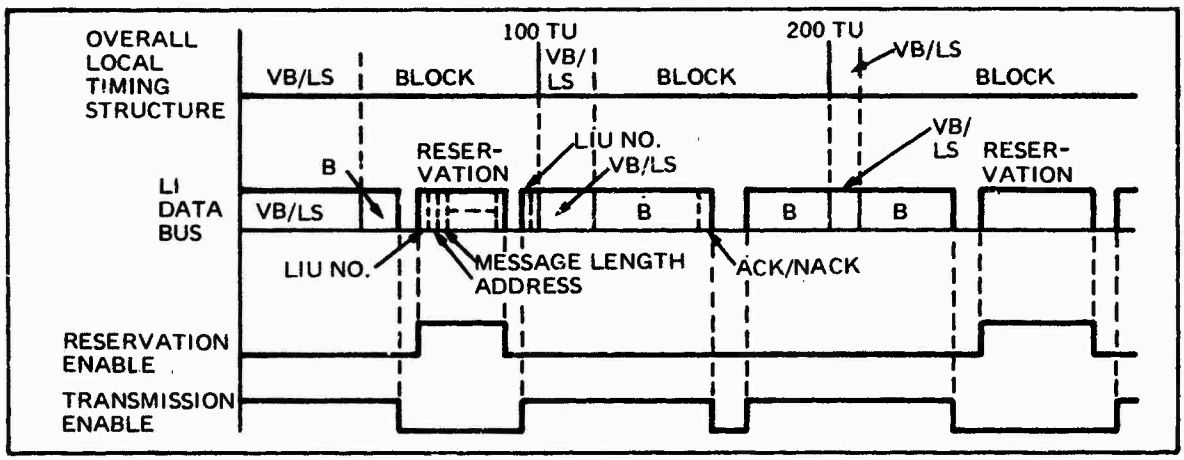


Figure 4.4.2-1. Timing of Local Data Bus and Transfer Control Bus. Using the data bus for message and reservation transfers, and a separate bus for control provides efficient data transfers as well as positive and flexible control of data flow.

3. CONTROL OF MESSAGES TRANSFERS ON THE LI

The local timing structure provides both control and data time slots, permitting reservations, handshake and data transmissions to be accomplished efficiently.

Local timing information is generated in the Local Intraconnect Control Unit (LICU). Each LIU and the EIU receives timing and control information and performs the processing necessary to participate in all local message transfer operations. The 18-bit data busses are bi-directional for transmission and reception in half duplex fashion. The control busses are uni-directional and most signals are generated in the LICU. Figure 4.4.3-1 identifies the data/control flow sequence.

The LIUs and the EIU continuously monitor the VB and LS slots using the number indicated by the control bus to determine the VB or LS bus number. Transmissions occur when the bus numbers and sequence numbers, preassigned to each LIU, appear on the control bus.

Time slots other than VB and LS slots are used for block message reservation or block message transfer according to control signals received from the LICU. When the reservation control is activated by the LICU, each LIU senses the reservation line and detects the word on the data lines for address matching. The polling address requires 6-bits; the remaining bits are used for indicating "this is the address polling word". If the address is matched, the LIU transmits the destination address and the message length using second and third word, respectively. (If no message is to be transmitted, it is so indicated in the second word.) The LICU may receive one or more reservations during each reservation period. Each reservation for point-to-point message transfer is examined against the destination memory status (stored in the LICU) for transmission front-end handshake. Memory status information is transmitted from each LIU and EIU periodically via memory status report lines in the control bus to the LICU. Message transfer is enabled only when the destination memory is available. (For broadcast messages, no front-end handshake is used.)

The combination of a deactivated reservation line and an activated transmission enable line indicates a Block message transfer period. Each LIU or EIU detects the transition of the transmission enable line from idle to active state and examines the data bus. The unit whose address matches the address on the data bus then transmits a Block message. The transmission enable line remains activated for a preset duration after the end of message to allow time for error checking by the receiving LIU. The last word of each transmission enable period is reserved for the ACK/NACK from the destination LIU. The source LIU receives the ACK/NACK and can determine if any further action is required.

In order to prevent bottlenecks at the EIU, the highest LI reservation priority is assigned to the EIU. This is achieved by using a dedicated reservation request line from the EIU to the LICU.

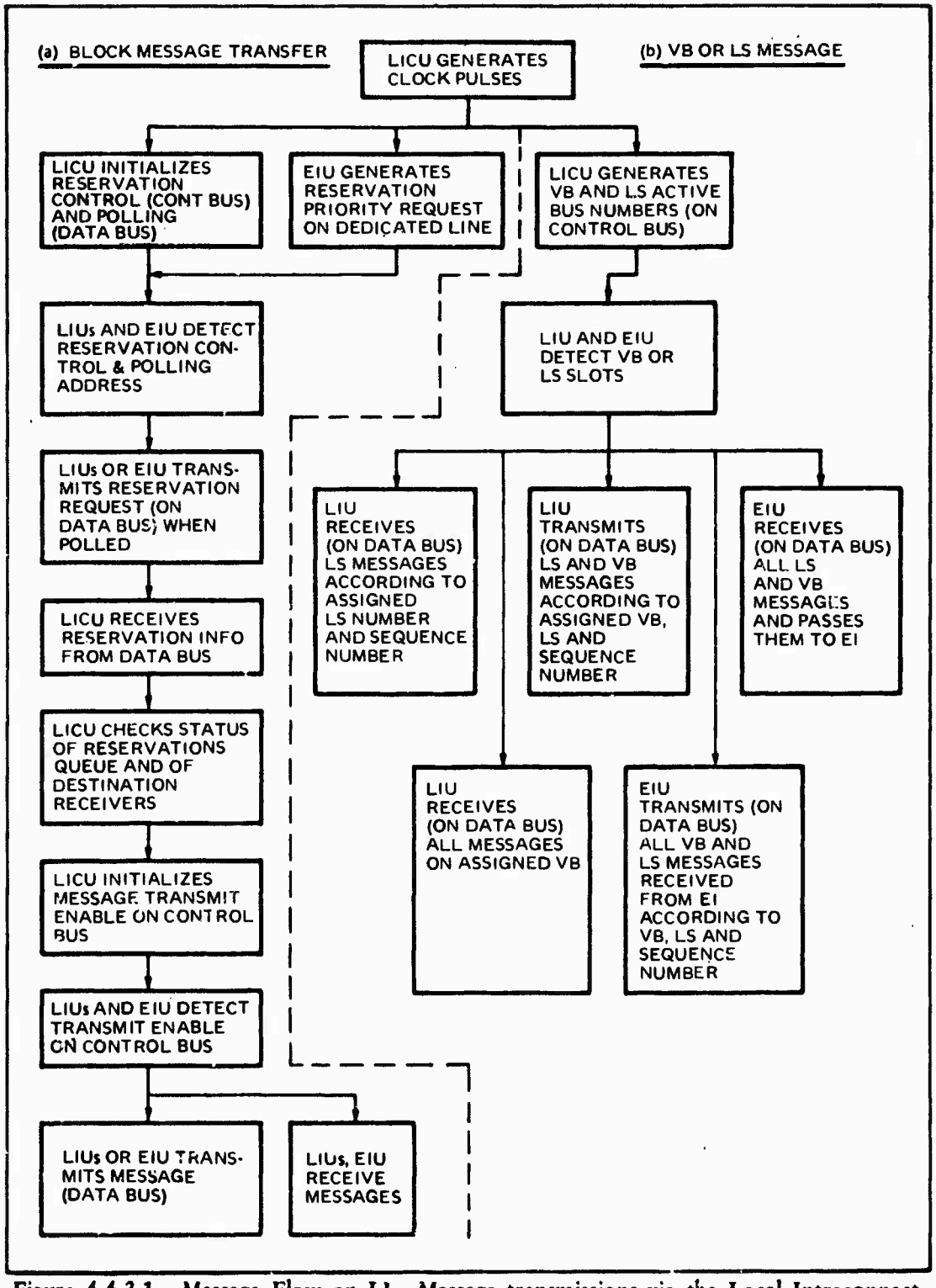


Figure 4.4.3-1. Message Flow on LI. Message transmissions via the Local Intraconnect result from the interaction of control signals transferred between the EIU, LIUs and the LICU over the data and control busses.

4. EXTERNAL TIMING STRUCTURE AND TRANSFER FORMAT

Reservation and handshake control bits are packed into the External Intraconnect time slot structure along with \B, LS and Block messages, providing an efficient means for distributed, positive control of message transfers.

Messages are transferred between shelters via the external intraconnect (EI). A number of timing constraints are imposed upon the design of this intraconnect: (1) timing must be designed to provide high transmission efficiency for the various types of messages, (2) bottlenecks which may cause EI saturation must be minimized and, (3) the timing structure must be capable of accommodating varying numbers of EIUs. It is desirable that the vulnerability resulting from centralized control be avoided, and finally, the timing structure must be capable of being reconfigured. Techniques have been developed which meet all these requirements.

Using fiber optic links, a communication range of 2 miles induces a propagation delay of 32 μsec. This delay could be compensated for by the use of guard bands of 32 μsec between each message, however this would severely reduce transmission efficiency and throughput. In the Hughes design, the need for propagation delay guard times is eliminated by compensating for the delay by advancing the start of the External Intraconnect time cycle in each EIU by an amount proportional to the propagation time to the end of the cable. All messages are then received in synchronism on the EI receive bus.

Figure 4.4.4-1, depicts the External Intraconnect time cycle in an FI configuration of 16 shelters. Block (B) messages, VB and LS message transfers, and transfer handshakes are packed in an orderly way in each cycle. 16 Short Block (SB) message slots are provided in the timing structure to accommodate 16 EIUs, (assuming each shelter is assigned one SB message slot).

The amount of time in each cycle allocated to transfers of block messages, Virtual Bus messages or Lazy Susan messages is variable and is determined by the application. For systems which make heavy use of the Virtual Bus and/or Lazy Susan feature, most of the cycle time is devoted to transferring those messages. However, the time needed to transfer one maximum length Block message (1024 18-bit words) is reserved. This time can be used to transmit many short messages, a few long messages, or one maximum length message.

A small portion of each cycle (about 4%) is devoted to the ACK/NACK and "front-end handshake" functions. The latter scheme contributes to the elimination of bottlenecks and provides high transmission efficiency. Front-end handshake is achieved through a three step process: (1) transfer of message counts between EIs, (2) requests for transfer of messages, and (3) the "granting" of such requests.

Each EIU is assigned a message count slot so that it can notify other EIUs as to the number of messages it desires to transmit during each cycle. The message count slots occur at the beginning of each cycle.

The next step in the front-end handshake process is issuance of transfer requests by EIUs desiring to transmit messages. The transfer request indicates the destination address and message length. (In the example in the figure, 40 slots have been allocated for this function). The third and final step is the transfer grant. These are replies from the destination EIUs which indicate readiness to accept messages. If the EIU memories are full, for example, it will not issue a transfer grant and the EIU desiring to transmit the message will not do so. In this way lost messages and the repeated transmission of lost messages are minimized. One transfer grant slot is required for each transfer request. (40 in the sample).

At the end of each cycle, slots are provided for the ACK/NACK. Performing ACK/NACK within the same cycle as the message transmission permits rapid indication of the status of the received message and avoids special handshake messages. Based on the design example as depicted in Figure 4.4.4-1, for a 1.0 μsec time unit (TU), the handshake portion (overhead) uses less than 5% of the total EI capacity.

The next topic describes the message transfer process in more detail.

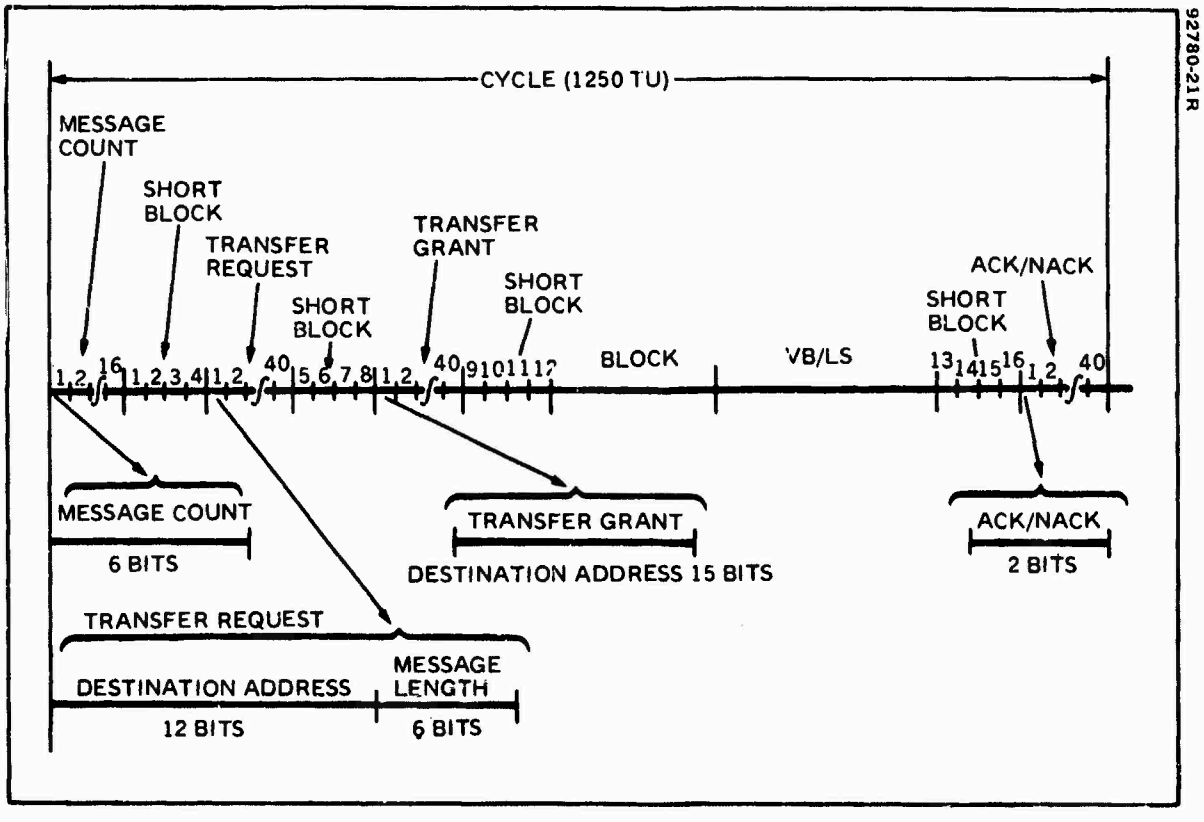


Figure 4.4.4-1. Structure of External Intraconnect Time Cycle. Allocating time periods for short messages between "handshake" slots provides fast response and eliminates the need for guard times.

5. MESSAGE TRANSFER SEQUENCE

Messages are transferred over the External Intraconnect only after a clear transmission path has been established. This is achieved by use of a reservation method implemented via a distributed control scheme.

The sequence of events in transferring messages over the external intraconnect is shown in the figure. As described in the preceding topic, a period of time is assigned to each EIU which enables it to inform all EIUs the number of messages it wishes to transmit. These "message counts" are transmitted at the beginning of each cycle. Each EIU receives these counts and therefore knows how many messages are to be transmitted during the cycle. While the count messages are being transferred to the EIUs (i.e., during the propagation delay time) SB messages can be transmitted.

Subsequent to the time allocated for the first series of SB messages, the EIUs detect their assigned transfer request slots and transmit transfer request messages. These are received by the addressed EIU which checks the status of its receive memory to determine if it can accept the message from the "sending" EIU. If it can, the destination EIU transmits a transfer grant for each message it can accept. The transfer grant contains a 15-bit field for the destination address and an indication to "send" or "don't send."

Again, in order that time not be wasted due to propagation delays, slots for SB messages are allocated both before and after the transfer request and transfer grant slots.

The Block messages for which transfer grants have been received are then transmitted in their appropriate reserved slots. Transfer of Block messages continues until interrupted by Virtual Bus and Lazy Susan time slots. After the EIUs transmit these two types of messages, and following another SB message period (compensating for propagation time) each EIU responds with an ACK or a NACK for each message for which a transfer grant was issued.

The above described process ensures that

- a clear transmission path has been established prior to start of message transfer
- each EIU is aware of the order and length of each message transmission

It should be noted that these characteristics are achieved in a highly responsive manner without wasting time waiting for propagation delays, and by means of a distributed (not centralized) control mechanism.

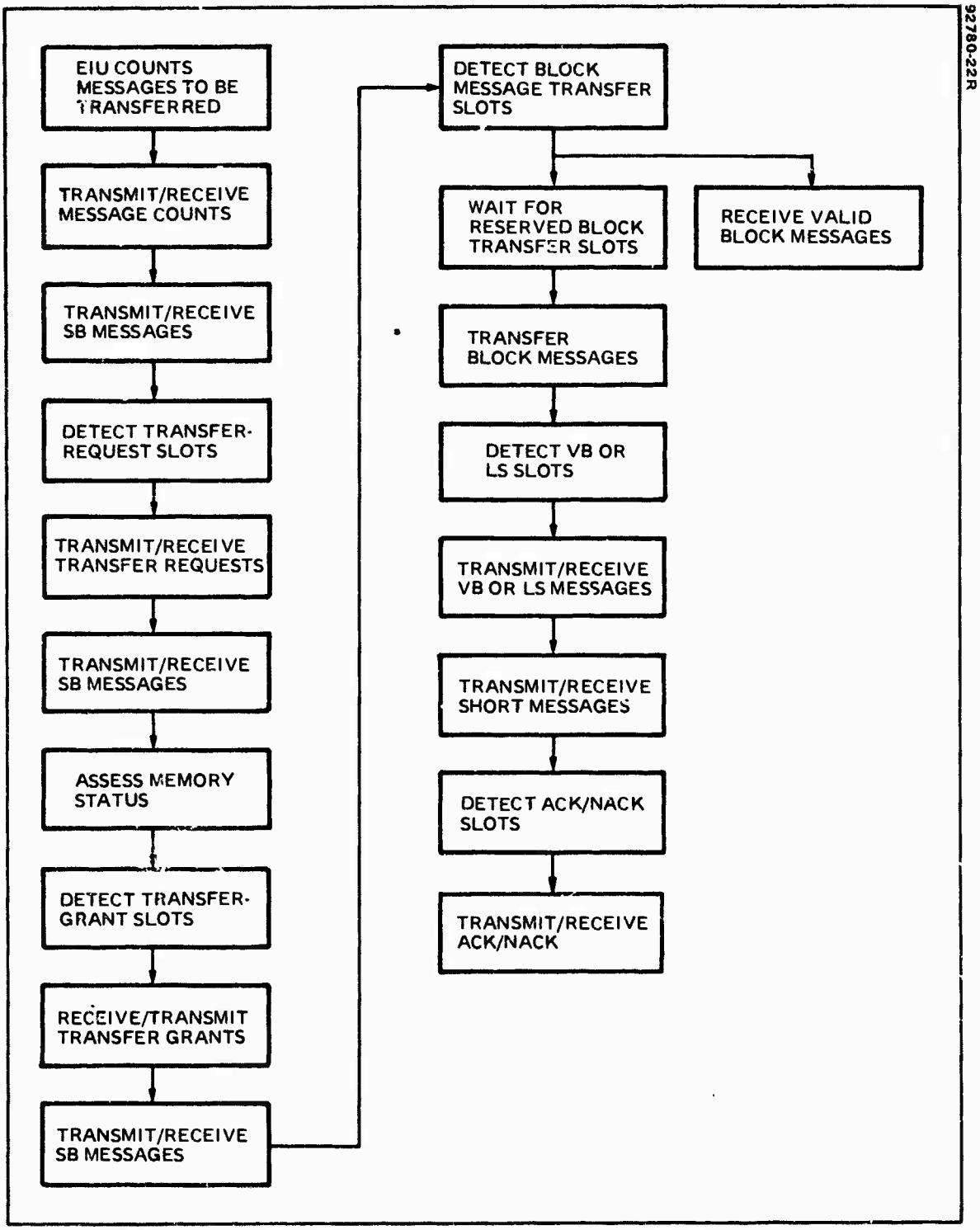


Figure 4.4.3-1. External Message Transfer Sequence. A distributed reservation control scheme provides for high transmission and efficiency and reduces bottlenecks.

6. EXTERNAL TIMING ACQUISITION ALTERNATIVES

Automatically switchable timing masters and "passive" master timing functions complement distributed control of the External Intraconnect. Epoch synchronization intervals are more efficient than message preamble synchronization procedures.

At the 20 Mb/s data rate per fiber (3 fibers @ 20 Mb/s = 60 Mb/s) timing accuracy is an important factor in reliable message reception. Each EIU has its own timing generator. Because all EIU timing must be constructed on a single timing base to assure a smooth and orderly data flow, the timing must be synchronized among the EIUs. Many timing acquisition approaches have been developed using open loop or closed loop procedures for this purpose.

In the open loop sync without a preamble, synchronization sequence is placed in front of each message transfer. The receiver detects the synchronization sequence to determine the message bit locations. Frequently the timing is refined via a tracking process. In closed loop sync methods timing is acquired via round trip transmissions. In this case, the timing is acquired prior to message transmission. In TDMA systems, the timing is often synchronized to a time reference and a preamble is used for each message transfer.

Open loop timing methods have the advantage of simple processing but generally provide low transfer efficiencies. The closed loop method requires more complicated processing and requires a reply from the "donor". For a TDMA system, a propagation delay guard time is generally provided, reducing transmission efficiency, or with a critical node (a relay) to eliminate the propagation guard time. The Hughes FI design with its external transmit and receive bus structure allows the use of a simple open loop timing acquisition procedure. Propagation guard time can be eliminated without creating a critical node.

A two step procedure is employed for EI timing acquisition: (1) epoch sequence synchronization and (2) loopback sequence synchronization. A timing master is also introduced as a timing reference. A 100 μs time duration is allocated in each 10 cycles for timing acquisition. This total time (10 cycles) is defined as an epoch. The 100μsec duration is further divided as depicted in the figure. At the beginning of the 100 μsec period, the master (any EIU) transmits a synchronization sequence called epoch sequence. Other EIUs initialize timing by switching to the listening mode. A correlation of the epoch sequence establishes an epoch timing mark. The master transmits an address code after the epoch sequence to poll an EIU for a loopback sequence transmission. A loop-back measurement period is provided the propagation delay from transmission to reception can be measured. The measured delay is then used to bias transmit timing to compensate for propagation delay. After the initial net entry timing acquisition, the epoch sequence can be used by EIUs for timing updates. Stability requirements of the EIU oscillators are not demanding. Based on a 1.25

msec cycle time and a 10 cycle epoch, a 10 nsec drift per epoch requires an oscillator stability of approximately 10^{-6}. A stability of 10^{-8} can be readily obtained using a temperature stabilized crystal oscillator.

Precautions against creating a critical node by the use of a master timing reference have also been taken. Every EIU can be a master. In case of failure, master functions are automatically taken over by the next backup EIU. Since the master function only involves a passive sequence and address transmission, a temporary failure does not interrupt FI communications.

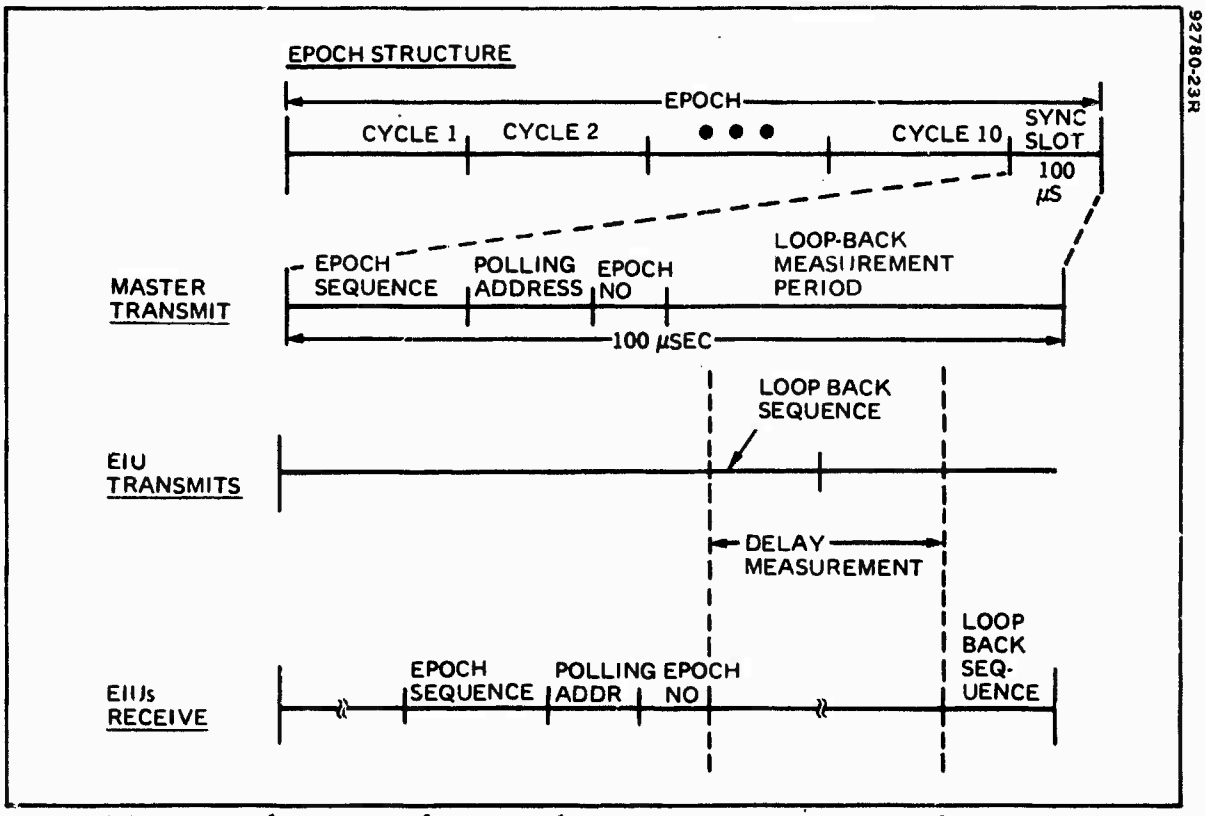


Figure 4.4.6-1. Epoch Structure for External Timing Acquisition. An epoch timing acquisition technique is used to measure propagation delay times.

7. TIMING ACQUISITION PROCEDURE

Timing acquisition by each EIU is a two step procedure which provides propagation time compensation without the use of guard times.

The two step timing acquisition (synchronization) procedure shown in Figure 4.4.7-1 establishes both reception and transmission timing. The first step, epoch sequence detection, is a passive sequence correlation for course synchronization. The second step, loopback sequence correlation, is a process for fine synchronization. Neither step requires responses from EIUs other than the master.

Epoch Sequence Detection – Timing acquisition is performed for each attempt of net entry. The EIU is normally set to receive data from the EI. The signal from the EI is continuously passed through a correlator where a correlation with a prestored epoch sequence reference takes place. Upon correlation the EIU examines the polling address and epoch number. (The polling address and the epoch number are incremented by one each epoch time.) After a preset N check, coarse synchronization which establishes basic receive timing is achieved.

Loopback Sequence Correlation – After coarse synchronization, the EIU continuously exams the polling address to locate the time for its loopback sequence transmission. The loopback sequence is transmitted and looped back to the receiving portion of the EI. The time difference between the transmission and reception is the propagation delay time. The epoch number and the delay measurement are then used for biasing the transmission time to compensate for the delay.

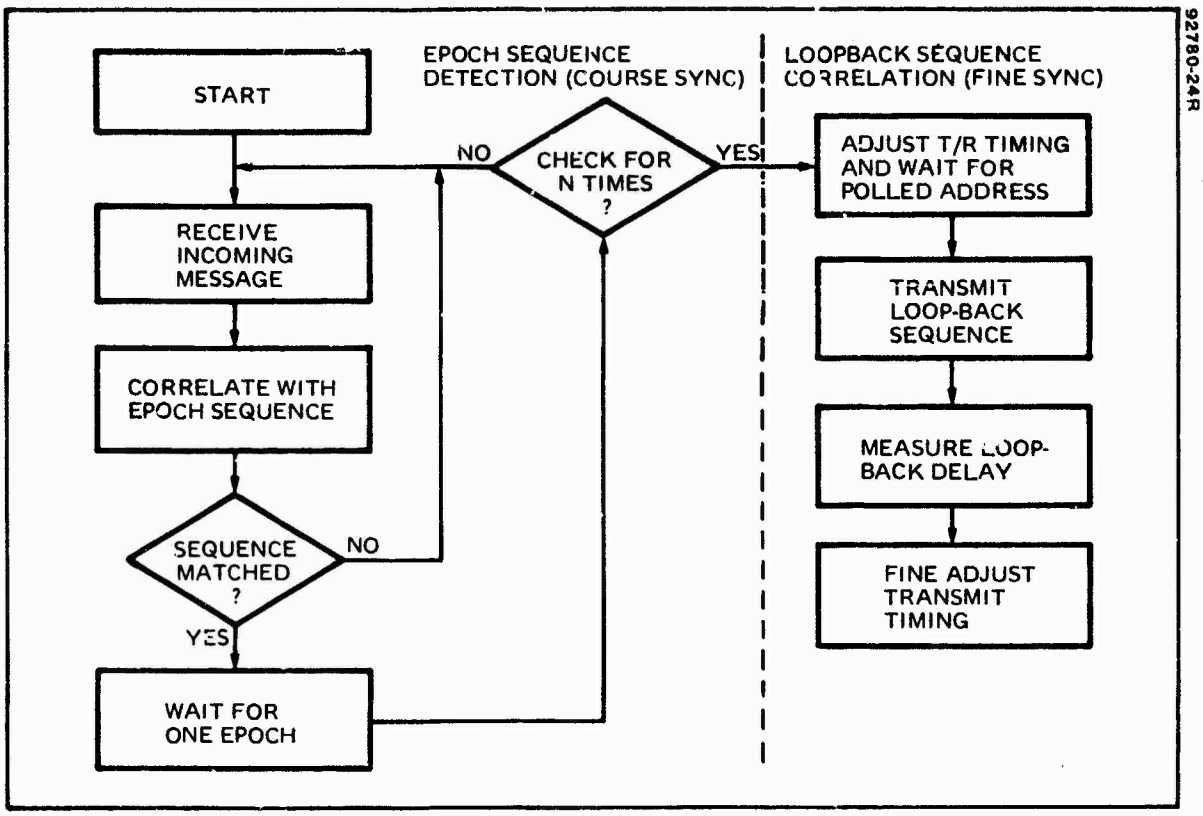


Figure 4.4.7-1. EIU Timing Acquisition. A simple two-step procedure establishes External Intraconnect transmit timing to compensate for propagation time.

SECTION 5
DESCRIPTION OF THE PREFERRED STANDARD INTERFACE

Part 1 – Task III, Preliminary Design Analysis
Section 5 = Preferred Standard Interface Description

1. PURPOSE AND BACKGROUND

A set of hardware and software standards termed the Preferred Standard Interface (PSI) has been developed for the FI/DTE interface. The PSI meets the needs of and promotes the further development of modular C^3 systems.

In the concept of modular communication, command, and control (modular C^3), every item of Data Terminal Equipment (DTE) utilizes the same data distribution system. The purpose of the Mod C^3 FI Analysis program is to develop such a data distribution system, known as the Flexible Intraconnect (FI). The FI design must offer extreme flexibility and a wide range of applicability. Instrumental to the flexibility and applicability of the FI is the FI/DTE interface. As a result of a 3-task study effort a PSI has been defined. It consists of a set of hardware interface and software standards.

In order to achieve long term flexibility and capability, a modular intraconnect system must have a generalized rather than a specialized design. Each intraconnect unit must be designed for full capability in order that each new application does not require a major redesign effort. In addition the FI must be capable of being configured and reconfigured in essentially an unlimited number of ways and in which DTEs may be attached to any FI outlet.

Several options were considered for the Preferred Standard Interface (PSI). Each option included a physical interface and a transfer protocol for that interface. The four options considered were the IBM 360/370 interface and protocol, the DEC PDP-11 interface and protocol, the Intel 8080A interface and protocol, and the Hughes AN/UYK-40 interface and protocol. The Intel 8080A option was selected because it is the simplest and is the most suitable for a Direct Memory Access (DMA) type of message transfer.

In the FI, and LIU interfaces directly with each DTE via the PSI. The Task 2 design specified that data be transferred across this interface in 9-bit halfwords. Depending on the direction of transfer, the LIU assembled 9-bit halfwords into 18-bit message words or the LIU disassembled the 18-bit message words into 9-bit halfwords. The LIU examined every halfword after each transfer to check for the end-of-message.

The message format consisted of a header section and a data section. The header section contained three 18 bit words. The words had various interpretations which depended on the message type. The data section contained up to 1024 (18 bit) data words, or 18-bit end-of-message word, and one 18-bit error check word.

In Task 3, the PSI concept of Task 2 was modified and developed further. The final PSI design is an asynchronous half duplex interface. It consists of 4 unidirectional control lines and 18 bidirectional data bus lines. The control line complement is minimal due to the protocol of message transfer and to the FI related control information in the message headers. Messages are

transferred in either full word segments over 18 data lines or in halfword segments over 9 data lines. The protocol of message transfer accepts a wide range of transfer rates from 180 megabits per second maximum to one word per 10 seconds, minimum.

The standard for the message format specifies a header section and a data section. The header section consists of 16 18-bit words. The information fields in the header have been defined so that each header word has only one interpretation. The data section consists of up to 1019 18-bit data words and 5 18-bit error check words.

All aspects of the PSI, including the message format, are described in greater detail in the five following topics.

TABLE 4.5.1-1. MAJOR ADVANTAGES OF THE PREFERRED STANDARD INTERFACE

- Supports a modular concept for C^3 Systems
- Accepts a wide range of user devices
- Allows rapid reconfiguration of system devices
- Allows for reassignment of functions among user devices

2. GENERAL DESCRIPTION OF THE PREFERRED STANDARD INTERFACE

The Preferred Standard Interface is a half-duplex interface featuring asynchronous data transfers using four control lines.

The Preferred Standard Interface (PSI) is the standardized interface between the Flexible Intraconnect (FI) system and the user devices. The Local Intraconnect Unit (LIU) interfaces directly with each DTE and provides the FI side of the PSI. The PSI, evolved from the Intel 8080A protocol, uses a bi-directional data bus and four uni-directional control lines to achieve positive handshake control of data transfer.

The PSI is a half-duplex interface. (See Figure 4.5.2-1.) Use of a full-duplex interface with bi-directional lines would require the DTEs and LIUs to examine each message word in order to determine the beginning and end of each message. The Output Data Request (ODR) and Input DATA Request (IDR) control lines establish the direction of each transfer, the start of each message, and the end of each message. In establishing the direction of transfer, ODR has priority over IDR. If the LIU activates ODR within two microseconds after the DTE activated IDR, the DTE yields to the LIU. The DTE monitors ODR and may not activate IDR while ODR is activated. Similarly, once the two microsecond period has passed, the LIU monitors IDR and may not activate ODR while IDR is activated.

When the direction of transfer and the beginning of the message are established, a message is transferred by changing logic levels on the remaining two uni-directional control lines. A message is transferred either in fullword segments over eighteen data lines or in halfword segments over nine data lines. The control lines accomplishing these full or halfword transfers are referred to by different names, depending upon the direction of message transfer. LIU Register Full/LIU Register Available (LRF/LRA), when referred to as LRF, indicates the LIU has a message segment on the data lines to transfer to the DTE. LRF/LRA, when referred to as LRA, indicates the LIU is available to accept a message segment from the DTE. DTE Register Full/DTE Register Available (DRF/DRA), when referred to as DRF, indicates the DTE has a message segment in the data lines to transfer to the LIU. DRF/DRA, when referred to as DRA, indicates the DTE is available to accept a message segment from the LIU.

Each word or halfword is asynchronously transferred via the PSI under positive control. A word or halfword is presented for transfer on the data lines when and only when the control signal from the receiving device indicates the input register of the receiver is not busy. After transfer occurs the receiver acknowledges acceptance of the data. Then, and only then, is the data cleared from the sender's output register. Whether the sender is the DTE or the LIU, the DTE always controls the instantaneous transfer rates.

An asynchronous transfer method was selected because it accommodates a wide range of devices and avoids dependency on timing or signal transitions which require close coupling and complex interface logic. Asynchronous transfers eliminate the wide variety of conditional control lines needed in a synchronous interface to meet the interrupt, signal conditioning, and software requirements of complex devices.

The maximum instantaneous transfer rate is ten megawords per second or twenty mega halfwords per second (180 megabits per second). The minimum instantaneous transfer rate is one word every ten seconds. The LIU is designed with this dynamic range in order to be compatible with the widest possible range of user digital devices.

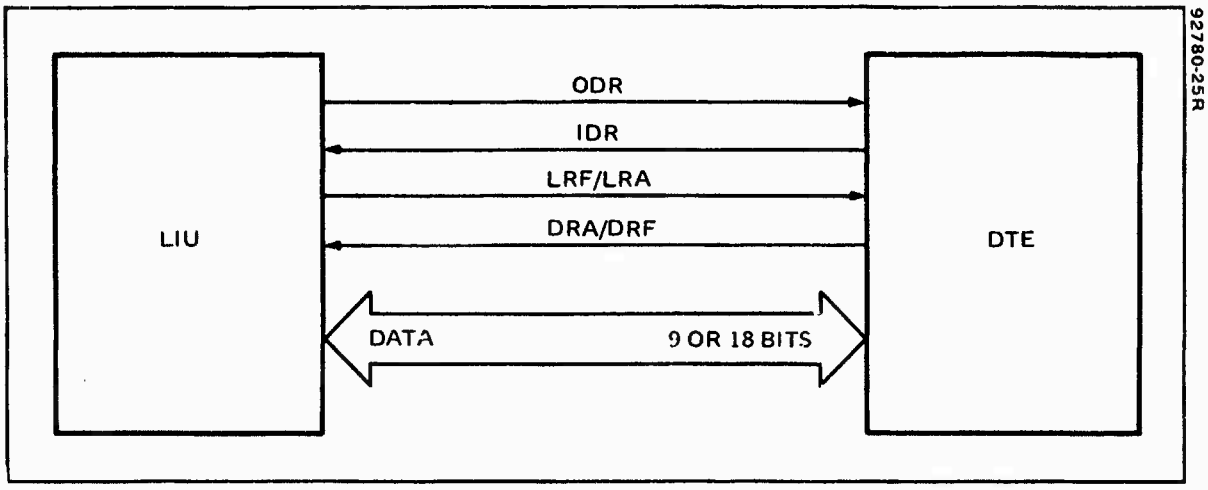


Figure 4.5.2-1. PSI Diagram. The PSI is implemented with 22 control and data lines providing disciplined, asynchronous transfer between the FI system and a wide range of user devices.

3. GENERAL DESCRIPTION OF MESSAGE STRUCTURE

All messages distributed by the FI conform to a standard format. Each message consists of a header section and a data section.

The header section always consists of 16 18-bit words. (See Figure 4.5.3-1.) It contains FI control information, FI provided service information, and a header error check word. The header error check word is a longitudinal parity check on the previous fifteen header words. Each header word has only one interpretation and is not applicable for every message type. Only the information fields in header words appropriate for a particular message type are filled in when the DTE generates the message and the FI modifies the message. The FI utilizes DTE-supplied information in the header to transfer data between DTEs.

The data section is composed of a data field and an error check field. The data field consists of up to 1019 18-bit words which are the information to be transferred. The error check field always consists of five 18-bit words, each of which is a longitudinal parity check on one-fifth of the words in the data field. The FI uses the error check field but does not modify any word in the data section.

Although the message format in general and the header section in particular are standardized, future adaptability is not restricted. As indicated in the figure, five header words remain undefined thereby allowing for the addition of new information fields. The addition of new information fields in the header, or a redefinition of existing information fields in the header, does not necessitate a redesign of the LIU since it is implemented with microprocessor technology rather than with hardwired dedicated logic. Modifications to the manner in which the LIU handles messages are accomplished by altering the software control programs resident in the LIU.

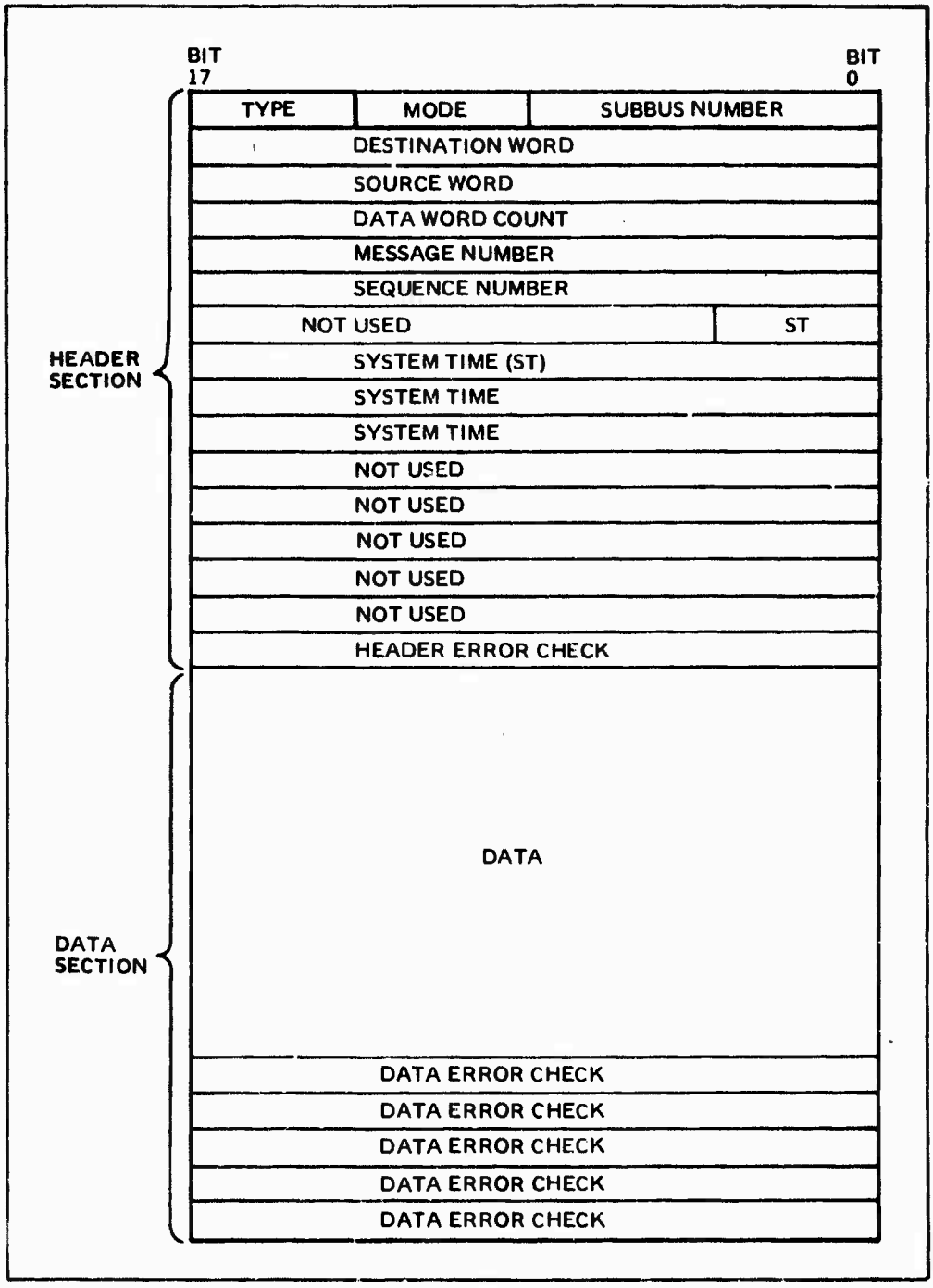


Figure 4.5.3-1. Message Structure. All messages distributed by the FI have two basic structural sections, the header and the data. The control information needed by the FI to perform its transfer functions is contained in the header.

4. HEADER FORMAT

The standardized header format specifies control information fields, service information fields, and an error check field. Not all information fields in the header are applicable for each message type.

The header section of the message contains 16 18-bit words. Each word consists of two 9-bit halfwords. In each halfword, the most significant bit is reserved for latitudinal parity, leaving a right-adjusted 8-bit information field. Thus, each header word contains two 8-bit information fields, with bits 17 and 8 of the word being used for latitudinal parity. Not all information fields are applicable for each message type. Various header words are utilized and/or modified by the FI. Other header words are not critical to FI operation and are strictly for the benefit of the DTEs using the FI system. The information bits for each of the 16 header words are specified below.

First Word – The first word has the following format:

Bit 17	Bit Ø
p tttt asss	p rrvv vvvv

Each halfword latitudinal parity (p) is a 1-bit field. The message type (t) is a 4 bit field. The message ACK/NACK (a) is a 1-bit field. The system mode (s) is a 3-bit field. The priority designation (r) is a 2-bit field. The Virtual Bus subbus number or Lazy Susan subbus number (v) is a 6-bit field. The subbus number ØØØØØØ is not valid.

The following message type (t) codes are defined: Ø11Ø for discrete messages, ØØ1Ø for local broadcast messages, ØØ11 for external broadcast messages, Ø1Ø1 for FI directed command messages, Ø1ØØ for DTE directed command messages, 1Ø1Ø for Virtual Bus messages, and 11ØØ for Lazy Susan messages. The LIU examines the message type (t) and the subbus number (v). No FI unit examines or modifies the message ACK/NACK (a), the system mode (s), the priority designation (r), and the halfword latitudinal parity (b).

Second Word – The second word has the following format:

Bit 17	Bit Ø
p fuww wwww	p uuxx xxxx

Each halfword latitudinal parity (p) is a 1-bit field. The destination External Intraconnect Unit (EIU) address (w) is a 6-bit field. The address ØØØØØØ is not valid. The destination LIU address (x) is a 6-bit field. The address ØØØØØØ is not valid. The address flag (f) is a 1-bit field. If the destination addresses used are FI defined real addresses, (f) is set to a logical one. If the destination addresses used are user defined virtual addresses, (f) is set to a logical zero. Three bits in the second header word are unused (u) and set to logical zero.

Word two recognizes the present design of 63 shelters with 1 EIU and 62 LIUs per shelter, while allowing for growth to 127 shelters with 1 EIU and 254 LIUs per shelter. The destination EIU address (w) and the destination LIU address (x) are specified for discrete and command messages. The LIU examines and modifies the destination address (w, x). The EIU examines the destination address (w). No FI unit examines or modifies the address flag (f) and the halfword latitudinal parity (p).

Third Word – The third word has the following format:

Bit 17	Bit Ø
p fuyy yyyy p uuzz zzzz	

Each halfword latitudinal parity (p) is a 1-bit field. The source EIU address (y) is a 6-bit field. The address ØØØØØØ is not valid. The source LIU address (z) is a 6-bit field. The address ØØØØØØ is not valid. The address flag (f) is a 1-bit field. If the source addresses used are FI defined real addresses, (f) is set to a logical one. If the source addresses used are user defined virtual addresses, (f) is set to a logical zero. Three bits in the third header word are unused (u) and set to logical zero.

Word three recognizes the present design of 63 shelters with 1 EIU and 62 LIUs per shelter, and allows for growth to 127 shelters with 1 EIU and 254 LIUs per shelter. The source EIU address (y) and the source LIU address (z) are specified for discrete, broadcast, command, Virtual Bus, and Lazy Susan messages. The LIU examines and modifies the source addresses (y, z).

Fourth Word – The fourth word has the following format:

Bit 17	Bit Ø
p cccc cccc p cccb dddd	

Each halfword latitudinal parity (p) is a 1-bit field. The data section word count (c) is an 11-bit field. The halfword mapping bit indicator (b) is a 1-bit field. If both halfwords are used in the last word of the data field, (b) is set to a logical zero. If only one halfword is used in the last data word, (b) is set to a logical one. When only one halfword is used, the left halfword (bits 17 through 9, inclusive) is used rather than the right halfword. The unused bit count (d) in the last data halfword is a 4-bit field.

The data section word count (c), the halfword mapping bit indicator (b), and the unused bit count (d) are specified for discrete, broadcast, command, Virtual Bus, and Lazy Susan messages. The LIU examines the data section word count (c). No FI unit examines or modifies the halfword mapping bit indicator (b), the unused bit count (d), and the halfword latitudinal parity (p).

Fifth Word – The fifth word has the following format:

Bit 17	Bit Ø
p mmmm mmmm p mmmm mmmm	

Each halfword latitudinal parity (p) is a 1-bit field. The message number (m) is a 16-bit field. The message number is a count per source per type of message.

4. HEADER FORMAT (Continued)

The LIU inserts the message number (m) into the header of discrete, broadcast, command, Virtual Bus, and Lazy Susan messages. No FI unit examines or modifies the halfword latitudinal parity (p).

Sixth Word – The sixth word has the following format:

Bit 17	Bit ∅
p qqqq qqqq p qqqq qqqq	

Each halfword latitudinal parity (p) is a 1-bit field. The sequence number (q) is a 16-bit field. The sequence number is a count maintained independently on each Virtual Bus and Lazy Susan subbus.

The LIU inserts the sequence number (a) into the header for Virtual Bus and Lazy Susan messages. No FI unit examines or modifies the halfword latitudinal parity (p).

Seventh Word – The seventh word has the following format:

Bit 17	Bit ∅
q uuuu uuuu p uuuu gggg	

Each halfword latitudinal parity (p) is a 1-bit field. System Time is measured in microseconds and represented by a 52-bit field. The seventh word contains the four most significant bits (g) of the System Time. Twelve bits in the seventh header word are unused (u) and set to logical zero.

The LIU inserts the System Time (g) into the header of discrete, broadcast, command, Virtual Bus, and Lazy Susan messages. No FI unit examines or

Eighth Word – The eighth word has the following format:

Bit 17	Bit ∅
p hhhh hhhh p hhhh hhhh	

Each halfword latitudinal parity (p) is a 1-bit field. The eighth word contains the 16 lower order bits (h) of the 20 most significant bits (g, h) of the system time.

The LIU inserts the System Time (h) into the header of discrete, broadcast, command, Virtual Bus, and Lazy Susan messages. No FI unit examines or modifies the halfword latitudinal parity (p).

Ninth Word – The ninth word has the following format:

Bit 17	Bit ∅
p jjjj jjjj p jjjj jjjj	

Each halfword latitudinal parity (p) is a 1-bit field. The ninth word contains the 16 higher order bits (j) of the 32 least significant bits (j, k) of the System Time.

The LIU inserts the System Time (j) into the header of discrete, broadcast, command, Virtual Bus, and Lazy Susan messages. No FI unit examines or modifies the halfword latitudinal parity (p).

Tenth Word – The tenth word has the following format:

Bit 17	Bit Ø
p kkkk kkkk p kkkk kkkk	

Each halfword latitudinal parity (p) is a 1-bit field. The tenth word contains the 16 least significant bits (k) of the System Time.

The LIU inserts the system time (k) into the header of discrete, broadcast, command, Virtual Bus, and Lazy Susan messages. No FI unit examines or modifies the halfword latitudinal parity (p).

Eleventh Word – The eleventh word has the following format:

Bit 17	Bit Ø
p ???? ???? p ???? ????	

Each halfword latitudinal parity (p) is a 1-bit field. The 16 information bits (?) of the eleventh word are unspecified and available for future use. When not in use, the bits are set to logical zero. No FI unit examines or modifies the unspecified bits (?) and the halfword latitudinal parity (p).

Twelfth Word – The twelfth word has the following format:

Bit 17	Bit Ø
p ???? ???? p ???? ????	

Each halfword latitudinal parity (p) is a 1-bit field. The 16 information bits (?) of the twelfth word are unspecified and available for future use. When not in use, the bits are set to logical zero. No FI unit examines or modifies the unspecified bits (?) and the halfword latitudinal parity (p).

Thirteenth Word – The thirteenth word has the following format:

p ???? ???? p ???? ????

Each halfword latitudinal parity (p) is a 1-bit field. The 16 information bits (?) of the thirteenth word are unspecified and available for future use. When not in use, the bits are set to logical zero. No FI unit examines or modifies the unspecified bits (?) and the halfword latitudinal parity (p).

Fourteenth Word – The fourteenth word has the following format:

Bit 17	Bit Ø
p ???? ???? p ???? ????	

Each halfword latitudinal parity (p) is a 1-bit field. The 16 information bits (?) of the fourteenth word are unspecified and available for future use. When not in use, the bits are set to logical zero. No FI unit examines or modifies the unspecified bits (?) and the halfword latitudinal parity (p).

Fifteenth Word – The fifteenth word has the following format:

Bit 17	Bit Ø
p ???? ???? p ???? ????	

Each halfword latitudinal parity (p) is a 1-bit field. The 16 information bits (?) of the fifteenth word are unspecified and available for future use. When not in use, the bits are set to logical zero. No FI unit examines or modifies the unspecified bits (?) and the halfward latitudinal parity (p).

Sixteenth Word – The sixteenth word has the following format:

Bit 17	Bit ø
e eeee eeee e eeee eeee	

The error check word (e) is an 18-bit field. This error check word is a longitudinal parity check on the previous fifteen header words.

The DTE supplies the error check (e) for all message types at the time of message generation. The LIU examines and modifies the error check (e).

Summary – In summary, the standardized header has the following format:

Word One	p tttt asss	p rrvv vvvv
Word Two	p fuww wwww	p uuxx xxxx
Word Three	p fuyy yyyy	p uuzz zzzz
Word Four	p cccc cccc	p cccb dddd
Word Five	p mmmm mmmm	p mmmm mmmm
Word Six	p qqqq qqqq	p qqqq qqqq
Word Seven	p uuuu uuuu	p uuuu gggg
Word Eight	p hhhh hhhh	p hhhh hhhh
Word Nine	p jjjj jjjj	p jjjj jjjj
Word Ten	p kkkk kkkk	p kkkk kkkk
Word Eleven	p ???? ????	p ???? ????
Word Twelve	p ???? ????	p ???? ????
Word Thirteen	p ???? ????	p ???? ????
Word Fourteen	p ???? ????	p ???? ????
Word Fifteen	p ???? ????	p ???? ????
Word Sixteen	c cccc cccc	c cccc cccc

5. CONTROL OF DTE TO LIU DATA TRANSFERS

In transfers to the LIU, the DTE both initiates transfers and controls the instantaneous transfer rate.

DTEs generate messages conforming to the standardized format of a header section and data section. The header section contains information needed to control distribution of the message once the message is in the LIU. Information in the header, however, is irrelevant to the methodology for transferring a message from the DTE to its associated LIU via the PSI. For transfer in this direction, three of the four uni-directional control lines in the PSI are applicable. These lines are Input Data Request (IDR), DTE Register Full (DRF), and LIU Register Available (LRA) (see Figure 4.5.5-1). In the quiescent state, all three of these control lines are negated.

The transfer methodology incorporates two levels of protocol. The first level of protocol governs the transfer of individual message segments (words or halfwords). The second level of protocol indicates message start and end. With this second level of protocol incorporated into the transfer methodology, the LIU does not need to examine each message segment to determine the beginning and end of the message.

The DTE initiates message transfer by asserting IDR (see Figure 4.5-4). This action established both the direction of transfer and the beginning of the message. The LIU does not respond to the asserted IDR if the LIU does not have memory space available for the maximum length message of 1024 18-bit words. If the LIU has the required memory space available, the message segments are transferred by changing logic levels on the DRF and LRA lines. All message segment transfers are identical, whether the transfer is the first one, the middle one, or the last one. Having identical message segment transfers eliminates the additional logic necessary to maintain a record of the progress of each message transfer and to initiate special sequences at appropriate times. (For the following discussion, a message transfer in full words segments is assumed. When a LIU is receiving halfword segments via the PSI, the LIU assembles the received halfword segments into full word segments.)

The LIU initiates a word transfer by asserting LRA (see Figure 4.5.5-2). The asserted LRA indicates that the LIU's input register is available. The DTE detects the asserted LRA and places a message word on the data lines. After the data lines have settled, the DTE asserts DRF. The LIU detects the asserted DRF, reads the data into its input register, and then acknowledges acceptance of the data by negating LRA. After the LIU has accepted the data, the DTE negates DRF and clears the data lines. This process repeats until all words within the message are transferred.

The LIU has a responsiveness equivalent to the maximum instantaneous transfer rate of ten megawords per second or twenty mega halfwords per second. The DTE therefore controls the instantaneous transfer rate by the rapidity with which it responds on DRF. The DTE instantaneous transfer rate may not exceed the LIU maximum and minimum limits.

After the last word is transferred, the DTE returns IDR to the negated state. This transition re-establishes the quiescent state and notifies the LIU of the end of the message. Again, this second level of protocol eliminates the need of the LIU to examine every message segment to determine the beginning and end of each message.

The transfer methodology discussed above is illustrated by a timing diagram in Figure 4.5.5-3. Individual transfer steps are represented by a control signal being negated or asserted to a stable logic level. Transfer steps are not a function of rise times or of pulsed signals. Thus, message transfer to a LIU is truly asynchronous.

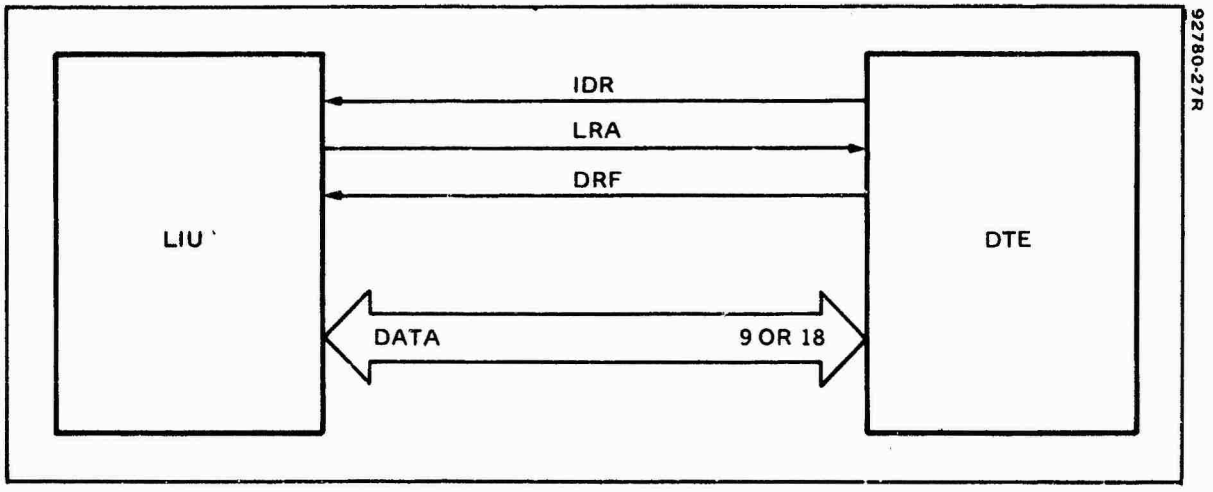


Figure 4.5.5-1. LIU Input From DTE: Applicable Signal Lines. Three of the four unidirectional PSI control lines are applicable to message transfer from DTE to LIU.

5. PROTOCOL OF LIU INPUT FROM DTE (Continued)

92780-28R

	ODR	IDR	LRA	DRF	
M_I	0	0	X	X	QUIESCENT
N		1	0	0	DTE HAS MESSAGE SEGMENTS TO TRANSFER
		1	1	0	LIU READY
		1	1	0	DTE PLACES A MESSAGE SEGMENT ON DATA LINES
		1	1	1	DATA LINES ARE VALID
		1	1	1	LIU READS DATA LINES
		1	0	1	LIU HAS ACCEPTED A MESSAGE SEGMENT
		1	0	0	DTE INDICATES END OF CURRENT MESSAGE SEGMENT TRANSFER
		1	0	0	DTE TESTS FOR END OF MESSAGE – NO, RETURN TO EVENT N – YES, GO TO EVENT M_{I+1}
M_{I+1}	0	0	0	0	QUIESCENT

Figure 4.5.5-2. LIU Input From DTE: Sequence of Events. The transfer methodology incorporates two levels of protocol. The first level governs the transfer of individual message segments. The second level of protocol governs the definition of an entire message transfer.

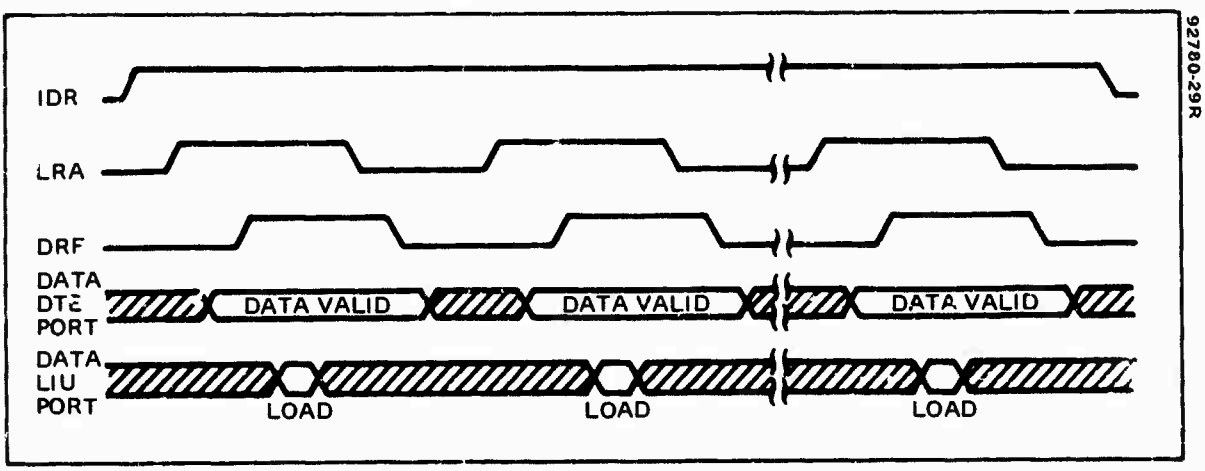


Figure 4.5.5 3. LIU Input From DTE FSI: Timing. All message segment transfers are identical, whether the transfer is the first one, the middle one, or the last one. Transfer events are not a function of rise times or of pulsed signals.

6. CONTROL OF LIU TO DTE DATA TRANSFERS

The same asynchronous transfer technique used for LIU input via the PSI is used for LIU output. In transfers to the DTE, the LIU initiates transfers but the DTE controls the instantaneous transfer rate.

Three of the four unidirectional control lines in the PSI are applicable to LIU to DTE data transfers. These lines are Output Data Request (ODR), LIU Register Full (LRF), and DTE Register Available (DRA) (see Figure 4.5.6-1). In the quiescent state, all three of these control lines are negated.

The transfer methodology for LIU output to DTE is the dual of the transfer methodology for LIU input from DTE (see Topic 4.5.5 of this document). Both processes require three control lines in the PSI. Two of these three control lines are common to both processes, but are referred to by different names. A third control line is unique to each process. In the case of LIU output to DTE, that third control line is ODR.

Being the dual of the input process, the transfer methodology for the output process incorporates the same two levels of protocol as the input process. The first level of protocol governs the transfer of individual message segments. The LRF and DRA control lines function at this level. The second level of protocol governs the definition of total message transfers. The ODR control line functions at this level.

The LIU initiates transfer by asserting ODR (see Figure 4.5.6-1). The asserted ODR establishes both the direction of transfer and the beginning of the message. After ODR is asserted, message segments (words and halfwords) changing logic levels on the DRA and LRF lines.

The DTE initiates a message segment transfer by asserting DRA (see Figure 4.5.6-2. The asserted DRA indicates that the DTE's input register is available. The LIU detects the asserted DRA and places a message segment on the data lines. After the data lines have settled, the LIU asserts LRF. The DTE detects the asserted LRF, reads the data into its input register, and then acknowledges acceptance of the data by negating DRA. After the DTE has accepted the data, the LIU negates LRF and clears the data lines. This process repeats until all message segments are transferred.

After the last message segment is transferred, the LIU returns ODR to the negated state. This transition reestablishes the quiescent state and notifies the DTE of the end of the message. This second level of protocol makes it unnecessary for the DTE to examine every message segment to determine the beginning and end of each message.

As in the input process, the DTE controls the instantaneous asynchronous transfer rate in the output process by the rapidity with which the DTE responds on DRA. The LIU always responds on LRF at the maximum limit. The DTE instantaneous transfer rate may not exceed the LIU maximum and minimum LIU limits.

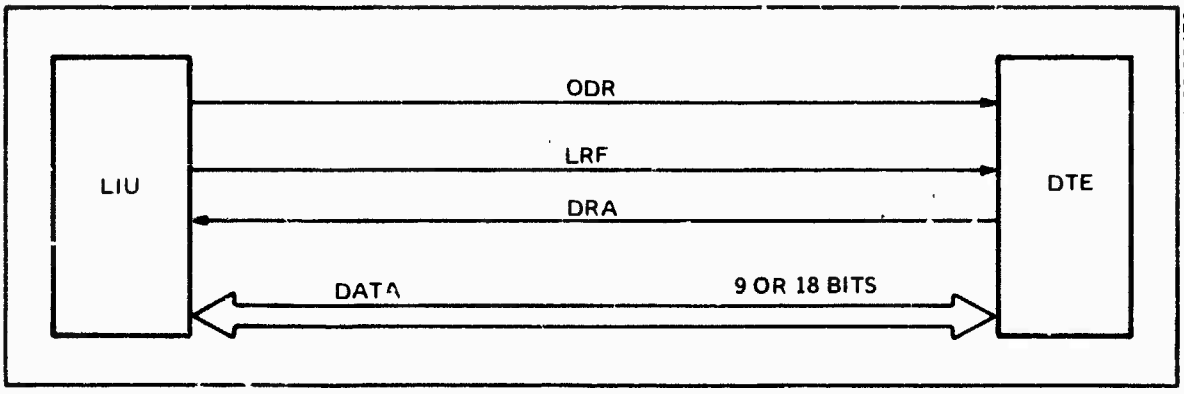


Figure 4.5.6-1. LIU Output to DTE: Applicable Signal Lines. Three of the four unidirectional PSI control lines are applicable to message transfer from LIU to DTE.

92780-31R

	ODR	IDR	LRF	DRA	
M_I	0	0	X	X	QUIESCENT
N	1		0	0	LIU HAS MESSAGE SEGMENTS TO TRANSFER
	1		0	0	DTE READY
	1		0	1	LIU PLACES A MESSAGE SEGMENT ON DATA LINES
	1		1	1	DATA LINES ARE VALID
	1		1	1	DTE READS DATA LINES
	1		1	0	DTE HAS ACCEPTED A MESSAGE SEGMENT
	1		0	0	LIU INDICATES END OF CURRENT MESSAGE SEGMENT TRANSFER
	1		0	0	LIU TESTS FOR END OF MESSAGE
					· NO, RETURN TO EVENT N
					· YES, GO TO EVENT $M_I + 1$
M_{I+1}	0	0	0	0	QUIESCENT

Figure 4.5.6-2. LIU Output to DTE: Sequence of Events. The transfer methodology incorporates two levels of protocol. The first level governs the transfer of indivisual message segments. The second level of protocol governs the definition of an entire message transfer.

SECTION 6
LOCAL INTRACONNECT UNIT DESCRIPTION

1. OVERVIEW OF LIU FUNCTIONS AND INTERFACES

The Local Intraconnect Unit is a standardized unit which adapts to a wide range of data terminal equipment characteristics.

Messages are input to the FI by a source DTE, routed internally by the FI, and then output from the FI to a destination DTE. The portion of the FI utilized in the process depends upon whether the communicating DTEs are in the same shelter or are in different shelters. The DTEs within the same shelter communicate with each other through their associated LIUs and via the LI (see Figure 4.6.A.1-1). The DTEs not installed in the same shelter communicate with each other through their associated LIUs and LIs, and via their shelter's EIU and the EI. For both intrashelter and intershelter communications, an LIU interfaces directly with each DTE and provides each DTE with access to the FI system.

Each LIU has three interfaces: PSI, LII, and CBI (see Figure 4.6.A.1-1). The PSI is the asynchronous, half-duplex interface between the LIU and its associated DTE; the LII is the full-duplex interface between the LIU and the LI; and the CBI is the interface between the LIU and the Control Bus.

Both the intrashelter and the intershelter communication processes result in four distinct transfer roles for every LIU. These four roles are: 1) LIU input from the DTE, 2) LIU output to the LI, 3) LIU input from the LI, and 4) LIU output to the DTE. At any instance, the LIU role depends upon whether its associated DTE is acting as a source or as a destination for the message being transferred.

The LIU processes each message in a manner depending upon the message type and the applicable LIU transfer role. Input from a DTE entails a sequence of steps consisting of message transfer, message checks, and message header modifications. The message checks ensure the validity of the message; the message modifications prepare the message for transmission to the LI.

Output to the LI consists of three transmission processes based on message type: Block (includes discrete, broadcast, command), VB, and LS. Each process handles placement of their respective messages on the LI.

Input to the LIU from the LI entails a sequence of steps consisting of message reception, message checks, and a message header modification. Three reception processes – Block, VB, and LS – handle removal of their respective messages from the LI. The message checks ensure the validity of the message; the message modification prepares the message for output to the DTE.

Output to a DTE consists of the message transfer and a transfer error check by the DTE. The methodology of message transfer for output to a DTE is the inverse of the methodology of message transfer for input from a DTE.

Key features of the LIU interface design are summarized in Table 4.6.A.1-1.

TABLE 4.6.A.1-1. KEY FEATURES OF THE LIU

- Presents standard interface to all devices
- Design independent of time slot configuration
- Microprocessor based message modification
- Segmentation of message memory prevents bottlenecks
- Header generation capability for simple DTEs

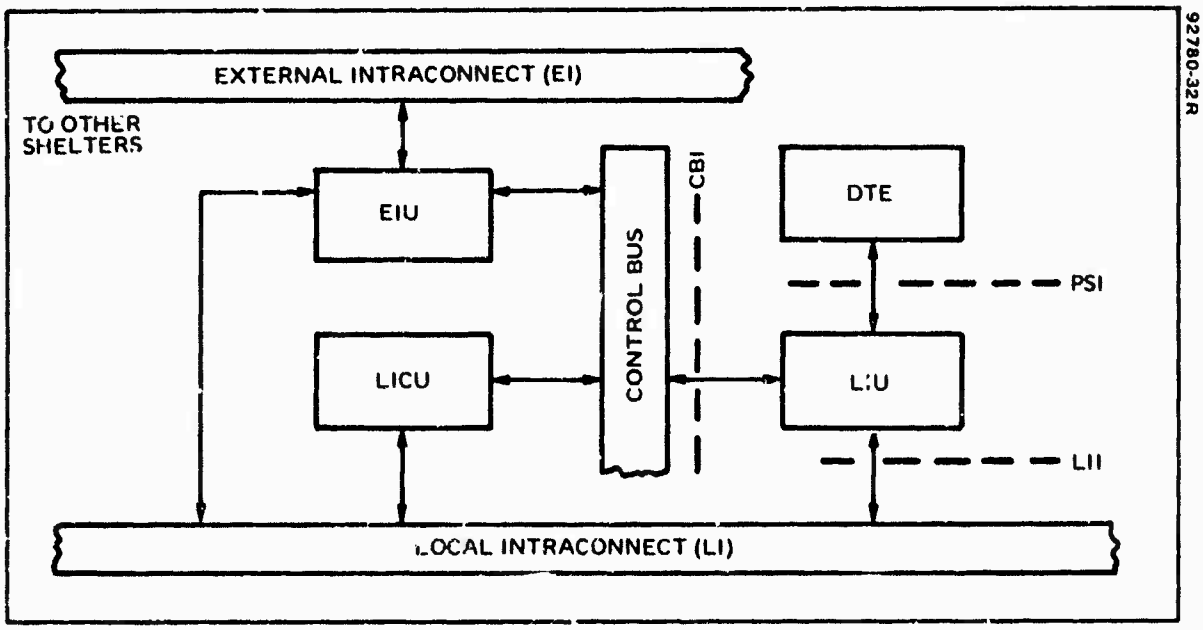


Figure 4.6.A.1-1. LIU and Its Interfaces. The LIU transmission and reception processes respond to timing and control information supplied by the LICU via the CBI. The LIU design is such that these processes operate independently of any particular LI time slot configuration.

2. MESSAGE FLOW THROUGH THE LIU

Segmentation of the LIU message store minimizes the occurrence of bottlenecks and provides efficient placement of messages on the LI.

The local intraconnect unit (LIU) message store is segmented into six portions. As shown in Figure 4.6.A.2-1, three of these portions contain messages which are waiting to be transferred to the LIU's associated DTE; the other three portions contain messages which are waiting to be transferred to other DTEs. The segmentation of the LIU message store minimizes bottlenecks on the local intraconnect (LI) and results in the efficient placement of messages on the LI.

Outgoing Messages – The DTE transfers messages to its associated LIU via the preferred standard interface (PSI). The LIU stores the message in one of three portions of the message store. Discrete, command, and broadcast messages are stored in the Block portion (see Figure 4.6.A.2-1) and the VB and LS messages are stored in their respective portions.

After storing the message the LIU performs several checks on and modifications to the message. The checks include a transfer error check, a message type check, and an authorization check. The modifications include a message number modification and a System Time modification. After the message passes all the checks and after all the modifications are completed, control of the message is handled by one of three transmission procedures available for placing messages on the LI. Messages in the Block portion of the LIU message store are distributed in the Block channel of the LI under control of Block transmission procedures. Messages in the VB portion of the LIU message store are distributed in the VB channel via VB transmission procedures and messages in the LS portion of the message store are distributed in the LS channel via LS transmission procedures.

Messages can be placed on the LI as the appropriate time slots become available, regardless of whether or not the transmission order is equivalent to the generation order of the messages.

Incoming Messages – The LIU examines the messages on the LI and removes those which are destined for its associated DTE via the LII. Incoming messages are placed in one of three portions of the LIU message store. Block messages from another DTE within the same shelter are placed in the local portion of the message store while Block messages from a DTE in a different shelter are placed in the external portion of the message store. With this arrangement, extensive reception activity by a LIU of local Block messages does not prevent that LIU from receiving external block messages. The VB and LS messages from DTEs in the same shelter or in a different shelter are placed in a common VB/LS portion of the message store.

The LIU continually reports to its LICU and EIU the status of the local and external portions of its message store. The LICU and EIU use this information for front-end handshake control to prevent bottlenecks in the Block message channel of the LI.

After the incoming message is stored in the appropriate portion of the message store, the LIU performs several checks on and a modification to the message header. The checks include a transfer error check, an authorization check, and a System Time check. The modification is an address conversion. After the message passes all the checks and after the modification is complete, control of the message is given to the PSI output procedure of the LIU.

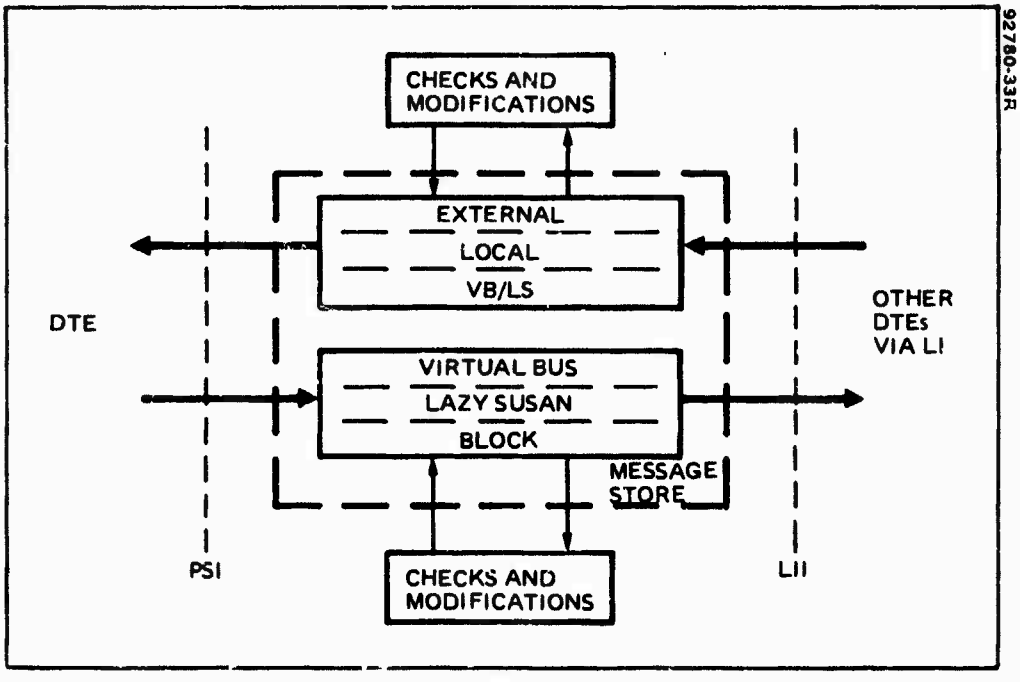


Figure 4.6.A.2-1. LIU Message Storage. Three segments of the LIU message store contain messages waiting to be transferred to the DTE; three segments contain messages waiting to be transferred to other DTEs via the LI.

3. THREE LIU INTERFACES

Each LIU has two interfaces for bilateral message transfer and one interface for receiving system timing information.

The PSI and the local intraconnect interface (LII) are the interfaces of the LIU over which messages are transferred. The Control Bus Interface (CBI) provides for the transmission of timing information (see Figure 4.6.A.3-1).

The PSI consists of four unidirectional control lines and eighteen bidirectional data lines. The unidirectional control lines are: 1) the output data request, 2) the input data request, 3) the LIU register full/LIU register available, and 4) the DTE register available/DTE register full. Efficient transfer of messages over the LIU-DTE interface with only four control lines is made possible by the message transfer protocol and by the control information present in message headers. (The PSI was discussed in Section 4.5.)

The LII consists of eighteen bidirectional data lines. It is each LIU's point of access to the LI. Timing information supplied to the LIU by the LICU via the CBI controls message transfer across the LII.

The CBI consists of unidirectional shared lines which include a Block message control bus (5 lines), a Virtual Bus/Lazy Susan (VB/LS) sub-bus identifier (7 lines), and clock pulses (4 lines).

The Block message control bus lines are memory status report sync, local memory status, external memory status, transmission enable, and reservation enable.

Memory status report sync, local memory status, and external memory status provide the LICU and EIU with information concerning the status of each LIU's message store. Continual monitoring of each LIU's message store enables front-end handshakes and prevents bottlenecks from forming in the Block channel of the LI. The reservation enable and transmission enable lines control time slot assignments and message transmission in the Block channel of the LI. The LICU first accepts reservation requests from LIUs and then enables each LIU's transmission at the correct time.

The seven VB/LS lines provide VB and LS timing information to each LIU. The logic levels are binary representations of the 63 distinct subbusses within either the VB channel or the LS channel of the LI. Transitions to stable logic levels on the VB/LS lines notify each LIU or VB and LS time slot boundaries.

Clock pulses supplied to the LIU include System Time (ST), word, cycle and epoch clocks. The system time line continuously supplies 1.0 microsecond clock pulses to every LIU within the shelter. Each LIU uses ST pulses to increment a 52-bit counter which represents system time. The word clock line continuously supplies a 5 Mhz signal to every LIU for LI synchronization. Cycle and epoch clocks aid VB/LS operations.

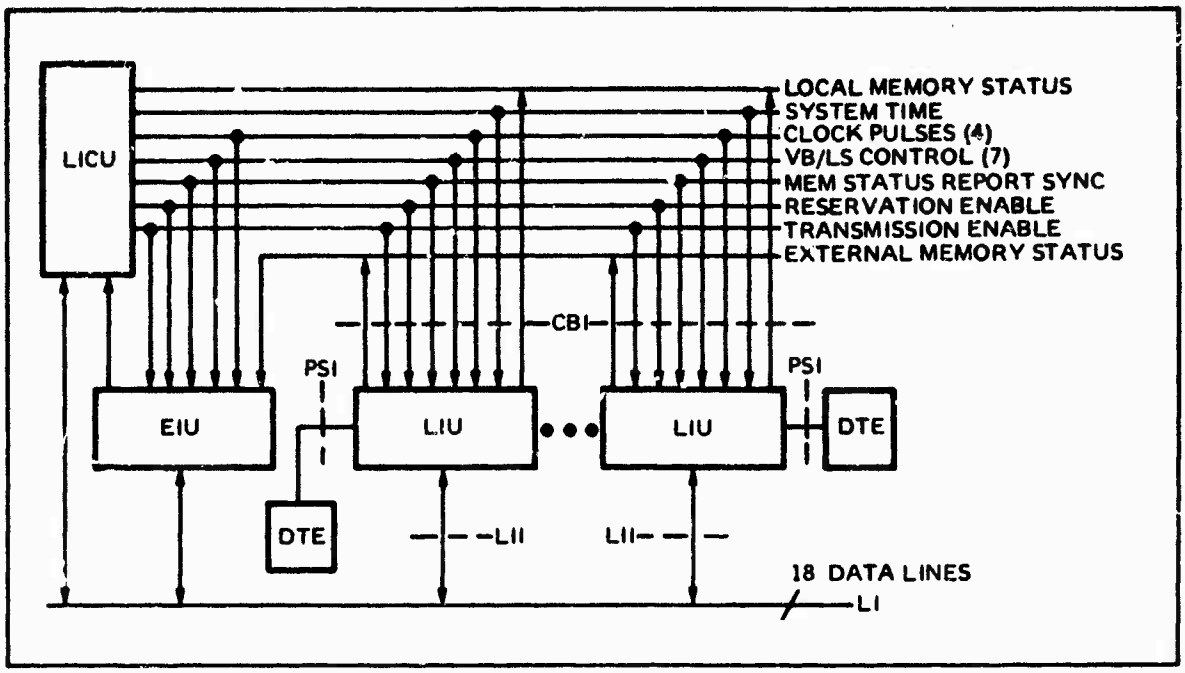


Figure 4.6.A.3-1. Control Bus Interface. The bus structure of the interfaces minimize LIU, EIU, and LICU hardware.

4. ERROR PROCESSING

The LIU generates error command messages for transmittal to the FI manager and to the responsible DTE upon detection of errors.

In processing messages for distribution over the LI or for transfer between it and its associated DTE, the LIU performs a number of error and authorization checks. In the event an error is discovered or an unacceptable message transfer is identified, the LIU inhibits the transfer and enters an error routine. This routine is illustrated in Figure 4.6.A.4-1.

The first step in the error routine is the generation of error command messages. Two situations exist: 1) the LIU detects an error or 2) a DTE detects an error and notifies its associated LIU of the error. In the former case, the LIU notifies both the FI manager and the DTE responsible. In the latter case, the LIU only notifies the FI manager. One error command message is generated for each party notified.

Rather than placing the burden of storing a summation table of errors for periodic reporting on each LIU, each error is reported so the FI manager has a current status of error conditions for the entire FI without the need for polling each LIU. Since the probability of error in the FI design is low, reporting each error individually does not significantly increase the FI traffic load.

Error command messages are generated immediately upon detection of the error or fault condition. However, these error command messages are not necessarily transferred to their destination immediately. Error command messages addressed to the LIU's associated DTE are placed in the local portion of the LIU message store. Error command messages addressed to the FI manager and to another DTE are both placed in the Block portion of the LIU message store. In all cases, the messages are placed in queue behind other messages already present in the respective portions of the message store.

After the error command messages have been generated and stored, the data message is erased in those cases in which the LIU detected the error and retransmitted in those cases in which the DTE detected the error.

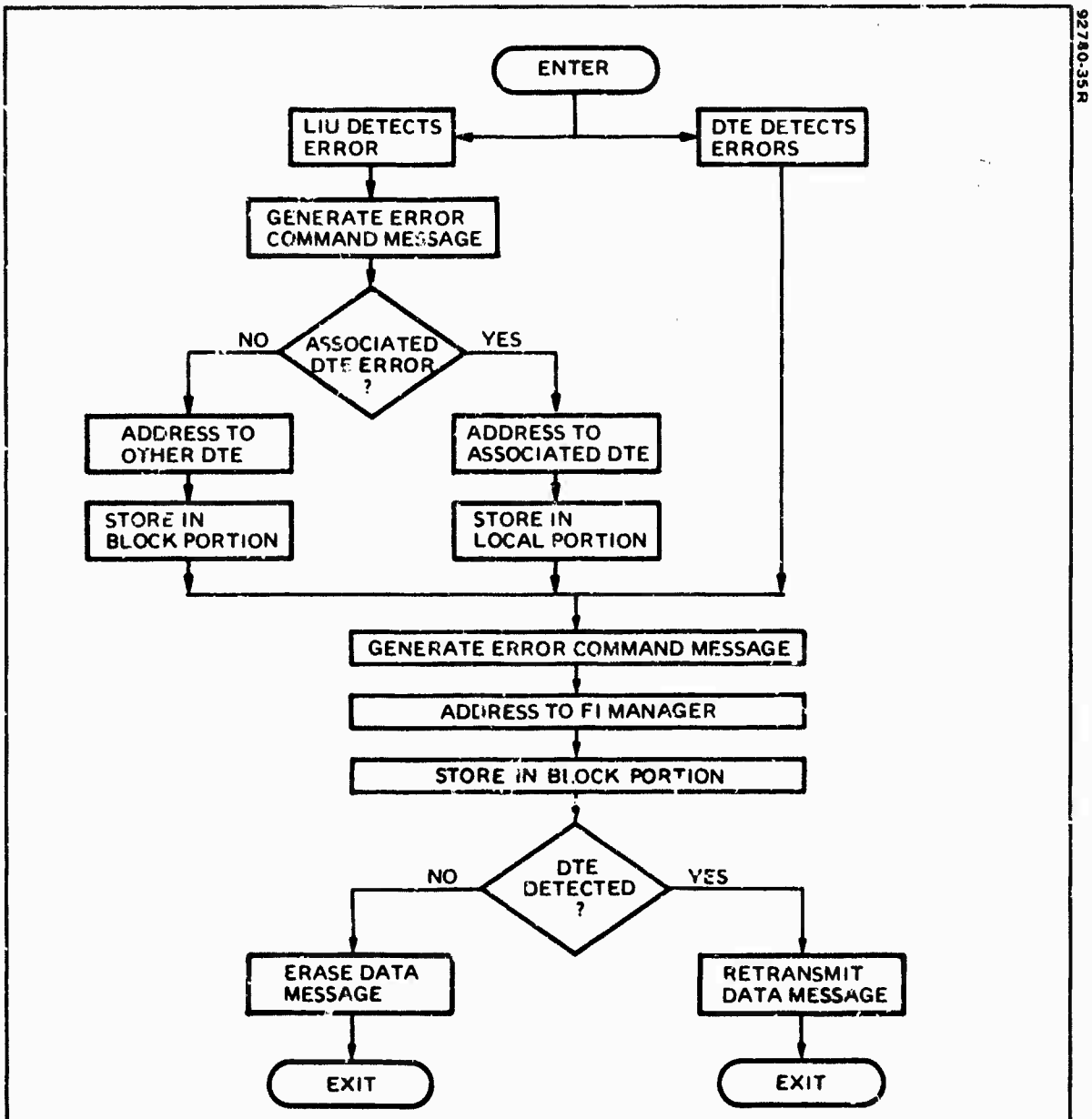


Figure 4.6.A.4-1. LIU Error Processing. The FI manager always has the current status of fault conditions in the entire FI since all errors are reported to the FI Manager as they occur.

Part 4 – Task III, Preliminary Design Analysis
Section 6 – Local Intraconnect Unit Description
Subsection B – DTE to LIU Data Transfers

1. CHARACTERISTICS OF MESSAGES FROM DTEs

It is the responsibility of the DTE to correctly format messages to be transmitted over the FI. However, provision has been made for the LIU to generate a prefix header when a DTE is incapable of this function.

Data terminal equipment (DTE) generate messages which are input to the FI at a source DTE, routed internally by the FI, and then output from the FI at a destination DTE.

In general, DTE generated messages are expected to conform to the PSI message standards which consists of a prescribed header section and a data section (see Figure 4.6.B.1-1). The header section contains 16 eighteen-bit words and the data section contains up to 1024 eighteen-bit words. The data section, which contains the information to be distributed, is of no concern to the FI. The header section, however, contains both FI related control information and FI provided service information (the message structure was discussed in detail in Topics 4.5.3 and 4.5.4).

Header information has two sources – FI related control information supplied by the DTE at the time of message generation and service information supplied by the local intraconnect unit (LIU) after the message has been transferred from the DTE. Each header word has a unique interpretation. (If multiple interpretations of the same header bit streams had been allowed, both the probability of misinterpretation of header information and the probability of incorrect distribution of messages would increase greatly.) Since all information fields are not applicable for each message type, a DTE fills in only those words which are appropriate. When generating discrete and command messages, the DTE must supply to the FI the message type (t), the external intraconnect unit (EIU) destination address (w), the LIU destination address (x), the EIU source address (y), the LIU source address (z), the data section word count (c), and the header error check word (e). When generating broadcast messages, the DTE must supply the message type (t), the EIU and LIU source address (y, z), the data section word count (c), and the header error check word (e). For Virtual Bus and Lazy Susan messages, the DTE must supply the message type (t), the subbus number (v), the EIU and LIU source addresses (y, z), and the header error check word (e).

When a DTE is incapable of generating a message which conforms to the PSI format, the LIU adds a prefix header section to the DTE supplied data message. This prefix header feature is discussed in further detail in Topic 4.6.B.2.

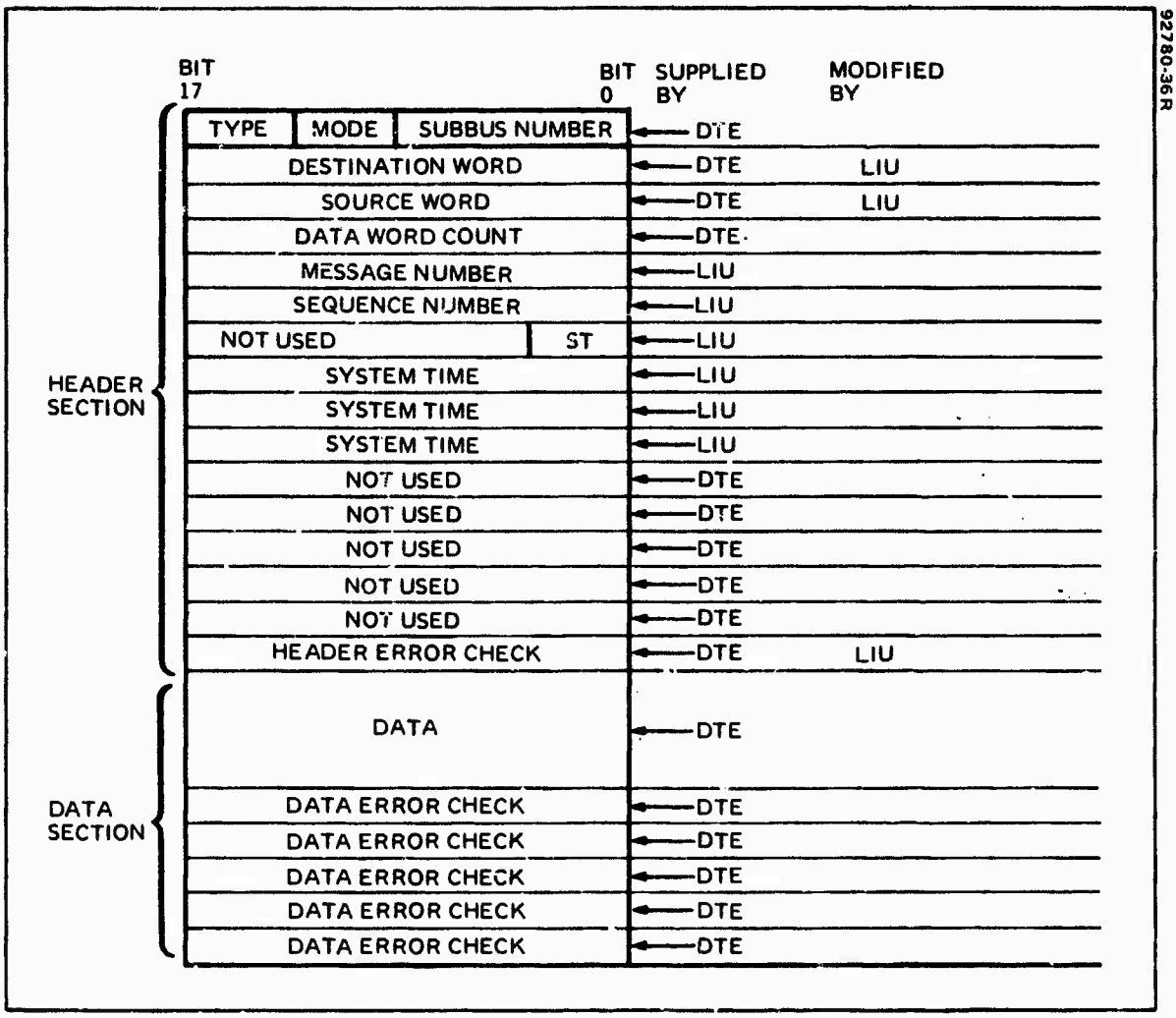


Figure 4.6.B.1-1. Sources of Information in Message Blocks. The header section contains both FI related control information and FI provided service information. The header information has two sources, but only one interpretation.

2. OVERVIEW OF TRANSFERS FROM DTE TO LIU

The LIU performs a series of checks on messages received from its DTE and prepares the message for transmission on the LI.

The LIU receives messages from its associated DTE via the PSI and prepares those messages for transmission on the LI. The LIU performs a series of checks on and modifications to each message received from the DTE (see Figure 4.6.B.2-1). Since the sequence of events is the same for all DTE messages (though not all events are applicable to every message type) a uniform LIU message processing cycle, maximum LIU efficiency, and minimum LIU logic requirements are achieved.

The message from the DTE is placed in store as described in topic 4.6.A.2. The LIU then executes checks on both the header and the data sections of the message and executes modifications to the header section. The first check is the input transfer error check which assures the accuracy of the FI related control information in the header and provides several data acceptance thresholds to the user. The next check is the message type check: discrete, command, broadcast, Virtual Bus, or Lazy Susan). The message type must be determined since subsequent checks and header modifications are based on message type.

The transmit address conversion function allows each user system on the FI to utilize his own "virtual" device addressing scheme independent of the FI "real" device addressing scheme. The LIU converts "virtual" addresses to "real" addresses by means of stored conversion tables.

The transmit authorization check prevents messages of an unauthorized DTE from being distributed by the FI. The LIU uses the "real" DTE address for this function.

Depending on the message type, the LIU inserts up to three pieces of service information into the message header: message number, sequence number and System Time. The message number is a tabulation by message type of the number of messages a DTE has generated. The sequence number is utilized to maintain transmission discipline on subbuses within the virtual bus and lazy susan channels. The system time is the time at completion of the majority of the header modifications. System Time is based on a universal time-date scheme. After insertion of the service information, the LIU recomputes the header longitudinal parity check word. The message is then sorted and placed under the control of the appropriate (Block, Virtual Bus, Lazy Susan) transmission procedure. Upon completion of this series of events, the message is certified as valid and is ready for transmission on the LI.

Message distribution by the FI depends upon header information. In order to provide for DTEs which cannot (or elect not) to generate headers, a prefix header function has been designed into the LIU. The LIU prefix header is initiated at the time of system initialization or during system reconfiguration

via command messages. Once the prefix header function is set, all data sections generated by the associated DTE receive a prefix header.

The data section generated by the DTE must be a fixed length block consisting of a data field and an error check field. The length of the data section is established at system initialization and at each system reconfiguration.

The correct prefix header, which was generated by either the user manager or the FI system manager, is stored in the LIU. (It may be for only one of the five message types.) Changing the prefix header stored in a LIU from one message type to another message type constitutes a reconfiguration of the LIU. After addition of the prefix header, LIU processing of the messages is indistinguishable from that of "normal" messages.

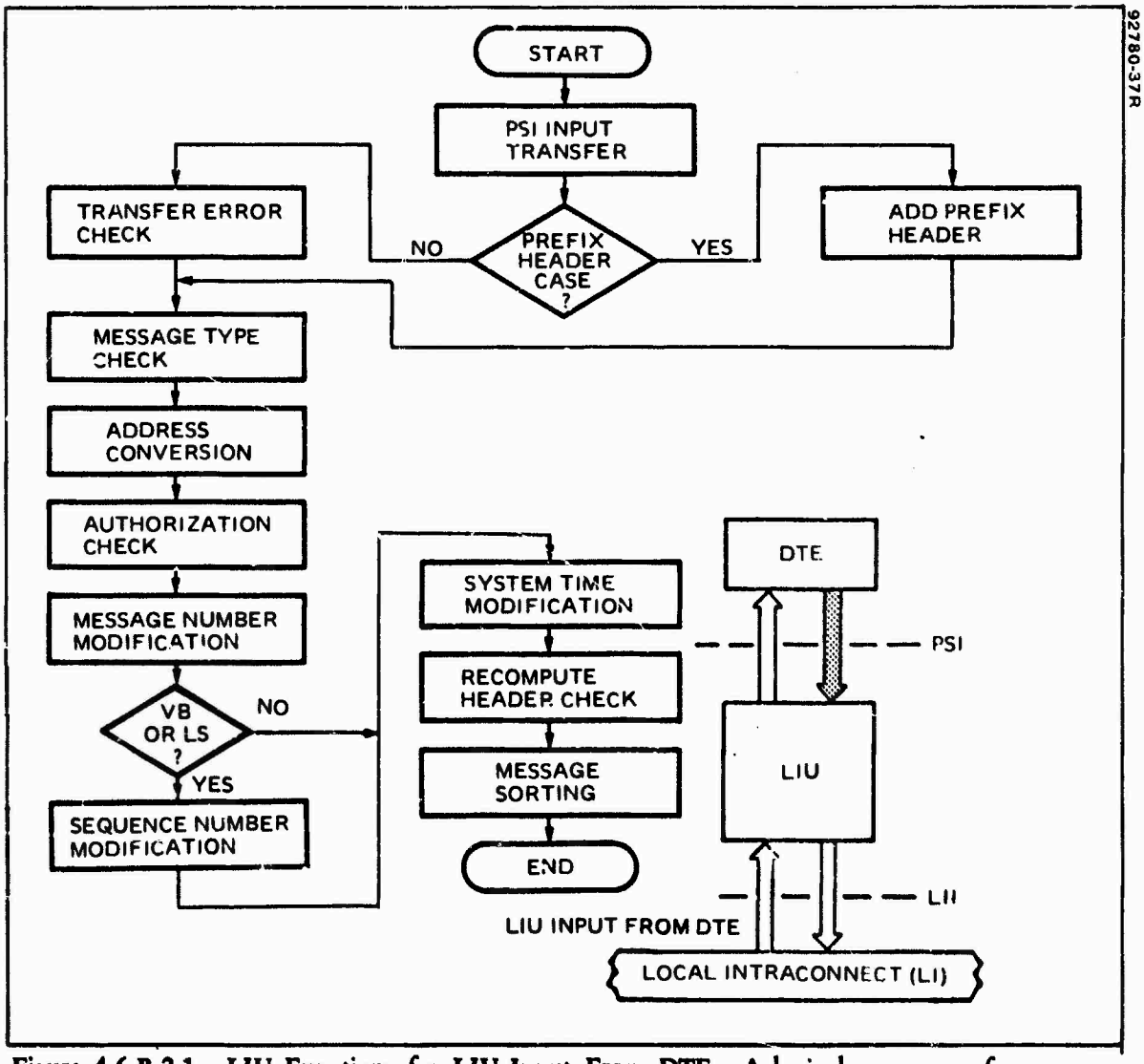


Figure 4.6.B.2-1. LIU Functions for LIU Input From DTE. A logical sequence of message transfers, message checks, and message modifications assures information accuracy and provides the DTE with status and control information.

3. TRANSFER OVER THE PSI

The DTE and LIU participate interactively in a standardized transfer methodology. Because of the extreme variances in DTE capabilities, the LIU rather than the DTE is responsible for maintaining discipline during these transfers.

The DTE transfers messages into the FI via the PSI. In addition to participating with the DTE in the standardized protocol of message transfer across the PSI, the LIU also performs several error monitoring functions.

Messages are transferred across the PSI in message segments (words, and half-words). The DTE establishes the beginning and end of message transfer by transitions to stable logic levels on the input data request (IDR) line. Each message segment is transferred by changing logic levels on the LIU register available (LRA) and the DTE register full (DRF) lines. The DTE controls the instantaneous transfer rate by the rapidity with which the DTE responds on DRF (see Figure 4.6.B.3-1). (The transfer methodology was discussed in detail in Section 4.5.5.)

A message is transferred either in full words over eighteen data lines or in half-words over nine data lines. In the following discussion transfer by half-words is called folded transfer; transfer by full word segments is called not folded transfer. When an LIU is receiving a folded message from its associated DTE, the LIU assembles the folded message into a not folded message. The decision to transfer folded or not folded messages across the PSI is not dynamic; that is, the folding decision is not made with every half-word message segment transfer or with every message transfer. The LIU logic assumes that transfers are folded unless notified otherwise during system initialization or during system reconfiguration by a command message.

The rate at which message segments (MS) are transferred is controlled by the DTE and monitored by the LIU. The DTE instantaneous transfer rate may not exceed the LIU maximum and minimum limits (ten megawords per second, twenty megahalf-words per second, and 1 word per 10 seconds, respectively). The rate monitor and pause monitor perform these checks. If the DTE exceeds these limits, the LIU initiates an error procedure.

The LIU also checks the message length. The maximum length message the LIU accepts is 1040 eighteen-bit words – 16 header words plus 1024 data words. If a DTE transfers more than 1040 eighteen-bit words in one message, the LIU initiates an error procedure.

During the error procedure for PSI input transfers, the LIU (1) generates an error command message addressed to the LIU's associated DTE which notifies the DTE that it must retransmit its message, (2) generates an error command message addressed to the FI manager which reports the type of error, and (3) erases the DTE message, whether the DTE message is partially complete or excessive in length. If the same type of error is repeated continuously, the LIU declares the PSI inoperative and notifies the FI Manager.

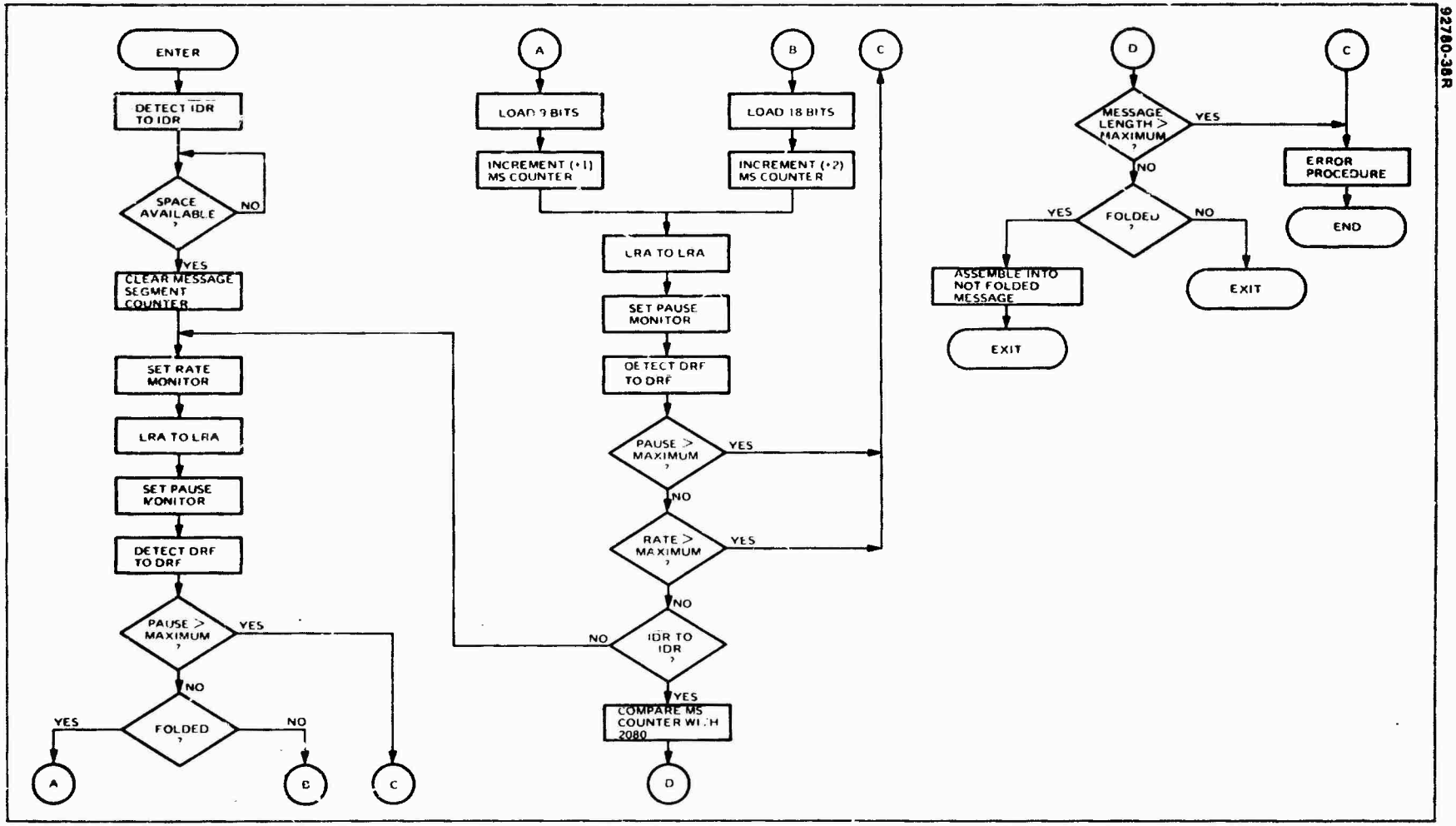


Figure 4.6.B.3-1. LIU View of PSI Input Transfer. The PSI input transfer is a DMA type transfer of a total message. Each message transfer consists of interactive asynchronous word transfers and several error monitoring functions.

When there are no errors in the transfer process, the DTE message is stored in successive memory locations of the LIU message store to await the performance of other checks and modifications. Upon completion of these checks and modifications, (described in the following topics) the message is placed on the LI for transmittal to its destination(s).

4. PSI INPUT TRANSFER ERROR CHECK

A header error check assures accuracy of FI related control information. Data acceptability is based on variable, but predetermined error rate thresholds.

Once the LIU has received an entire message from the DTE, the LIU performs a longitudinal parity check on both the header and the data section of the message (see Figure 4.6.B.4-1).

The error check on the header section consists of two parts. First, the LIU computes a longitudinal parity check on the first fifteen header words. The LIU then compares the error check word it computed with the error check word (16th word) it received in the message header section. If the parity bits match, the header is assumed to be correct. If there is any discrepancy between the computed and received parity bits, the LIU initiates an error procedure.

Whereas the threshold for header acceptance is absolute, the threshold for data acceptance is programmable. The data error rate acceptance threshold that the LIU must recognize is placed in the LIU at the time of system initialization or during system reconfiguration via a command message. The command message can be originated by the FI Manager, by the LIU's associated DTE, or by another DTE already operating on the FI.

The error check on the data section is also a longitudinal parity check. The data section contains five error check words, each of which is a longitudinal parity check on one-fifth of the words in the data field (see discussion of error rate analysis). The LIU compares its computed error check words with the received error check words in the data section. If the number of detected errors exceeds the established limit, the LIU initiates an error procedure.

During the error procedure for PSI transfer error check, the LIU (1) generates an error command message addressed to the LIU's associated DTE which notifies the DTE that it must retransmit its message, (2) generates an error command message addressed to the FI Manager which reports a message did not pass the parity check, and (3) erases the erroneous DTE message.

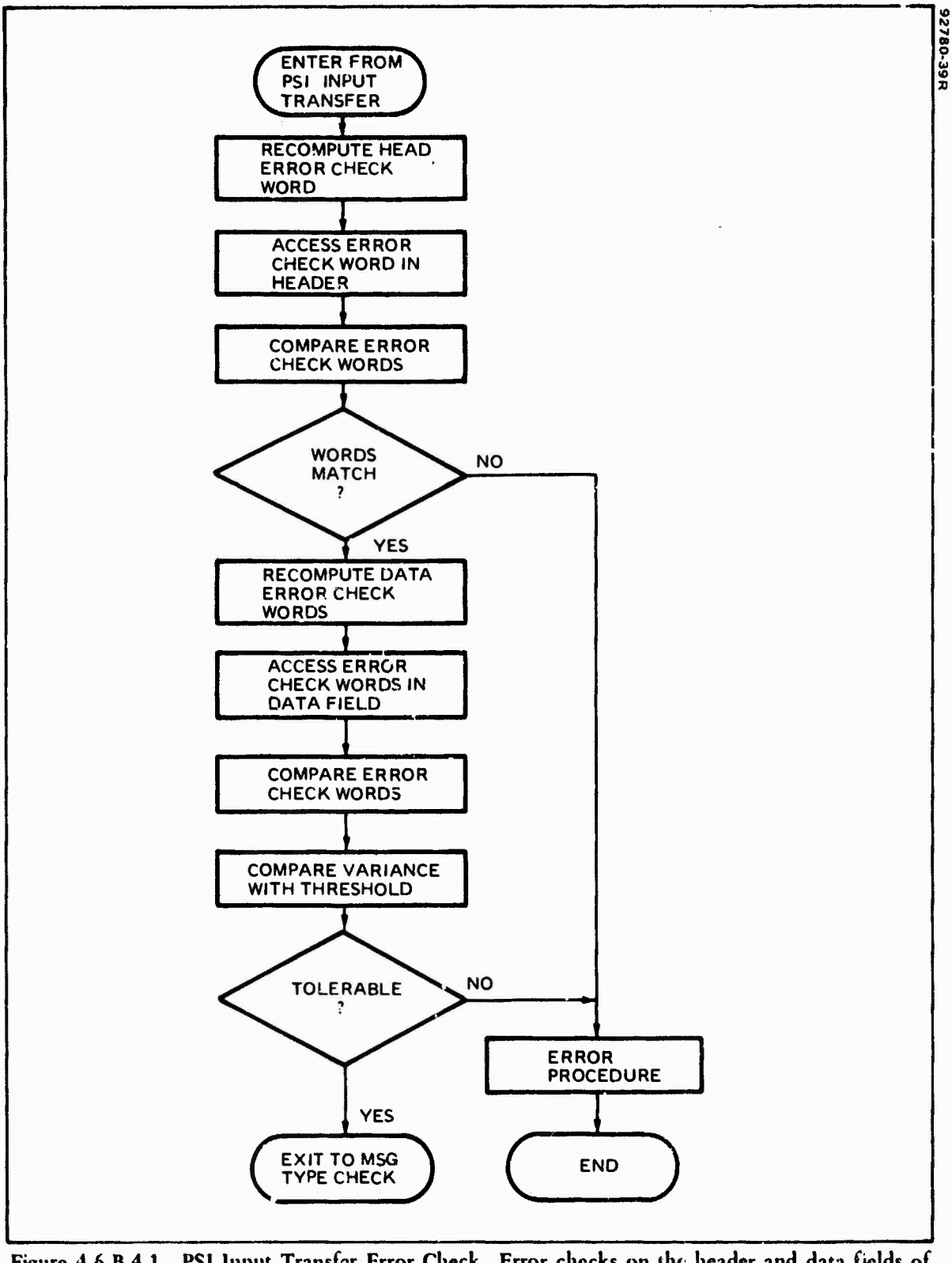


Figure 4.6.B.4-1. PSI Input Transfer Error Check. Error checks on the header and data fields of messages prevents the FI from accepting, processing, and distributing erroneous information.

5. DETERMINATION OF MESSAGE TYPE

Each LIU accepts up to five types and subtypes of messages based on instructions from the FI Manager.

The FI distributes five kinds of messages: discrete, command, broadcast, Virtual bus, and Lazy Susan. The first three are types of Block messages. The FI Manager defines valid codes for each of these message types and places a list of the valid message type codes in every LIU during system initialization or reconfiguration.

Each LIU uses this list of valid message type codes stored in its random access memory to determine if the DTE is using a valid code and, if so, which one. Prior to transmitting a message on the LI and after receiving a message from the LI, the LIU must determine the type of message since subsequent checks and modifications are different for each message type.

The first word of each message header contains a DTE supplied message type code (t). The LIU correlates the type code in the message header with its own list of valid type codes (see Figure 4.6.B.5-1). If the correlation is not successful, the LIU initiates an error procedure. If the correlation is successful, the LIU sets processing flags. Based on the processing flags, the LIU selects subsequent message processing functions. (For example, the sequence number modification is applicable to Virtual Bus messages, but not to discrete messages).

During the error procedure for the message type determination, the LIU (1) generates an error command message addressed to the LIU's associated DTE which notifies the DTE that it must use the proper type codes in order for its messages to be processed and transmitted, (2) generates an error command message addressed to the FI Manager which reports on invalid message type code in the DTE message, and (3) erases the erroneous DTE message.

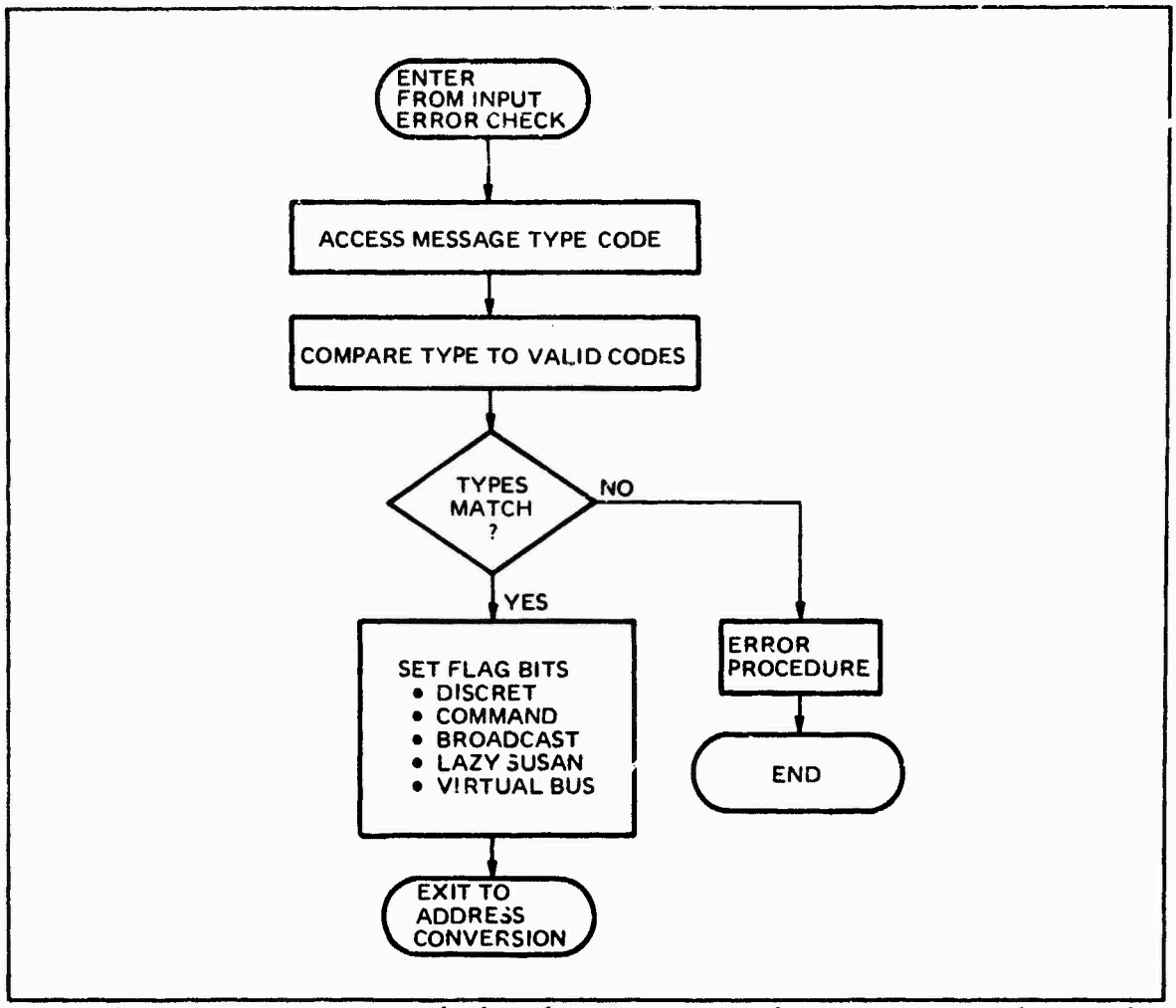


Figure 4.6.B.5-1. Message Type Check. The LIU examines the message type codes in order to select the subsequent message processing functions.

6. TRANSMIT ADDRESS CONVERSION

The address conversion function allows each DTE on the FI to use its own addressing scheme independent of the FI addressing scheme.

Depending on the message type, when the DTE generates a message it specifies either (1) the External Intraconnect Unit (EIU) destination address (w) and the LIU destination address (x), or (2) the EIU source address (y) and the LIU source address (z), or (3) both. The EIU and LIU addresses used by the FI to distribute messages are called real addresses. The addresses used by the DTE are called virtual addresses. The DTE defined virtual addresses may or may not match the FI defined real address.

The FI defined addressing scheme is standardized. The FI contains a maximum of 63 shelters, each with 1 EIU and a maximum of 62 LIUs for a total of 3906 addressable locations. Each EIU address is a six-bit field and each LIU address is a six-bit field. A particular source or destination is specified by both an EIU address and an LIU address. Each EIU and LIU is notified of its real address when the FI is initialized or reconfigured. When DTEs use virtual addresses, the source LIU converts the user defined virtual addresses to the FI defined real addresses prior to transmitting a message on the LI. The destination LIU does the reverse conversion after receiving a message from the LI. The conversion to real addresses is necessary since several of the checks the LIU performs are based on these addresses.

Each LIU has an address conversion table stored in random access memory (RAM). This table is for discrete, command, and broadcast messages. (No address conversions are necessary for Virtual bus and Lazy susan messages since checks on these types of messages are based on the sub-bus number.) The destination address (w, x) is removed from the second word of the message header, converted using the table, and replaced in the header (see Figure 4.6.B.6-1). The source address (y, z) located in the third word of the message header, is converted in the same way. If the real address counterpart to the virtual address in the message header is not present in the RAM, the LIU initiates an error procedure.

During the error procedure for the transmit address conversion, the LIU (1) generates an error command message addressed to the LIU's associated DTE which notifies the DTE that either the DTE must obtain for its LIU all necessary virtual/real address pairs or the DTE must use only real addresses, (2) generates an error command message addressed to the FI Manager which reports that the LIU does not have the real address counterpart for a particular virtual address, and (3) erases the erroneous DTE message.

The use of the virtual addressing scheme permits DTE movement since such movement will be invisible to other DTEs: that is, a DTE can be moved from one FI shelter to another FI shelter without affecting the DTE's addressing scheme. The FI Manager simply updates the address conversion tables in the appropriate LIUs.

The table of virtual/real address pairs is placed in the LIU's RAM during initialization or reconfiguration by command messages.

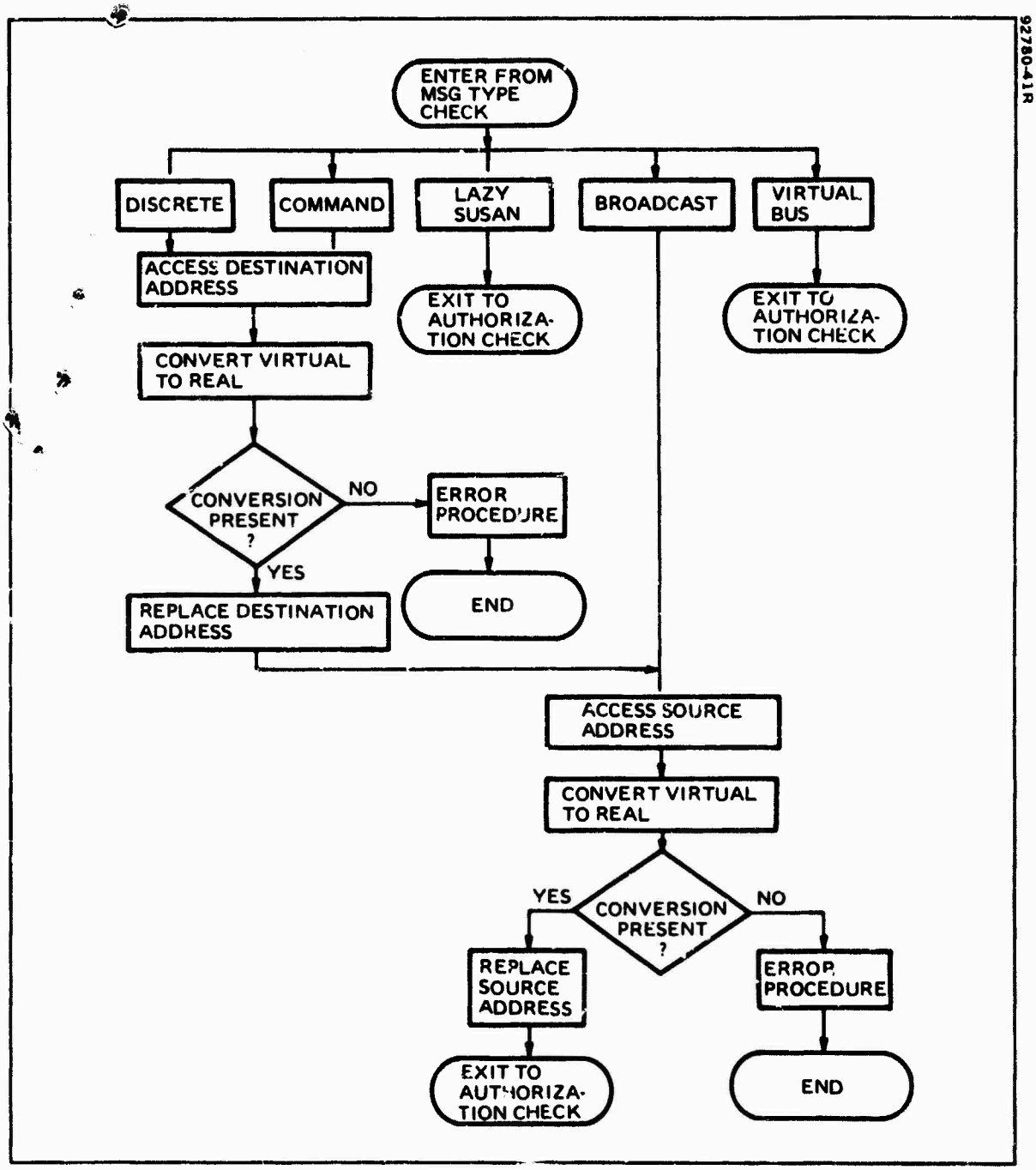


Figure 4.6.B.6-1. Transmit Address Conversion. Depending on the message type, either the source address, the destination address, or both, are converted from a user defined virtual address to a FI defined real address.

7. TRANSMIT AUTHORIZATION CHECK

The transmit authorization check prevents messages from an unauthorized DTE from being distributed by the FI system.

The authorization check function is based on authorization tables. Each group of DTEs using the FI system sets up authorization tables for its member DTEs. These authorization tables are stored in the LIU. There are several authorization tables since the authorization for each message type is different (see Figure 4.6.B.7-1). For discrete and command messages, the LIU accesses the destination address (w, x) in the DTE message header. For broadcast messages the LIU accesses the source address (y, z); for Virtual Bus and Lazy Susan messages, the LIU accesses the subbus number (v).

For discrete and command messages, a DTE is only authorized to transmit to a specific set of other DTEs. Only authorized destination addresses that a source DTE is allowed to transmit to are contained in the authorization table. (Since a user system may define its own virtual addressing scheme, the LIU always performs the authorization check for these message types on the FI defined real addresses.) The LIU correlates the destination address (w, x) with destination addresses in the authorization table. If the destination address in the message header matches a destination address in the table, the message is authorized to be transmitted. If the destination address in the message header does not match destination addresses in the table, the discrete or command message is not transmitted and the LIU initiates the error procedure.

Local broadcast messages are authorized separately from external broadcast messages. The LIU reads the source address (y, z) in the third word of the message header and compares it with the source address in the authorization table. If source address in the message header matches the source address in the table, the message is broadcast. If the source address in the message header does not match the source address in the table, or if the table does not contain the LIU source address, message transmission is inhibited and the LIU initiates an error procedure.

A DTE is only authorized to transmit Virtual Bus and Lazy Susan messages on specified subbuses. Numbers of these subbuses are contained in the authorization table. The LIU performs the authorization check by comparing the subbus number (v) in the first word of the message header with the subbus numbers in the authorization table. If they match the message is transmitted. If the subbus number in the message header does not match any subbus number in the table, the DTE message is not transmitted and the LIU initiates the error procedure.

During the error procedure for the transmit authorization check, the LIU (1) generates an error command message addressed to the LIU's associated DTE which notifies the DTE that it must request a change in its authorization environment, (2) generates an error command message addressed to the FI

Manager which reports an attempted use at an unauthorized environment; and (3) erases the erroneous DTE message.

The LIU table of authorized addresses and sub-bus numbers is placed in RAM in the LIU during initialization. After initialization, addresses and sub-bus numbers can be added to and deleted from the table via command messages. The command messages can be originated only by the user group manager or the FI Manager. A DTE may not establish its own authorization tables.

For discrete, broadcast, and command messages, the authorization check function can be implemented jointly with the address conversion function. The virtual address is used as the memory address. The real address for that virtual address and an authorization flag bit are stored in the memory location given by the virtual address. If the flag bit is asserted and if the real address is present, the message is authorized and the real address is inserted into the message header. If the flag bit is negated, then regardless of whether or not the real address is present, the message is not authorized and the LIU initiates an error procedure. With this method, only one memory access is required to perform two functions, thereby minimizing LIU memory requirements and LIU message processing time.

For Virtual Bus and Lazy Susan messages, the authorization check functions are implemented in a similar fashion. The sub-bus number and one additional address bit are used as a memory address. The additional address bit distinguishes between the Virtual Bus and Lazy Susan channels. The sub-bus number then specifies one of the sixty-three sub-buses in either the Virtual Bus or Lazy Susan channel. Each memory location specified by the sub-bus number and the channel address bit contains an authorization flag bit. If the flag bit is asserted, the DTE is authorized to transmit on that sub-bus in that channel. If the flag bit is negated, the DTE is not authorized to transmit and the LIU initiates an error procedure.

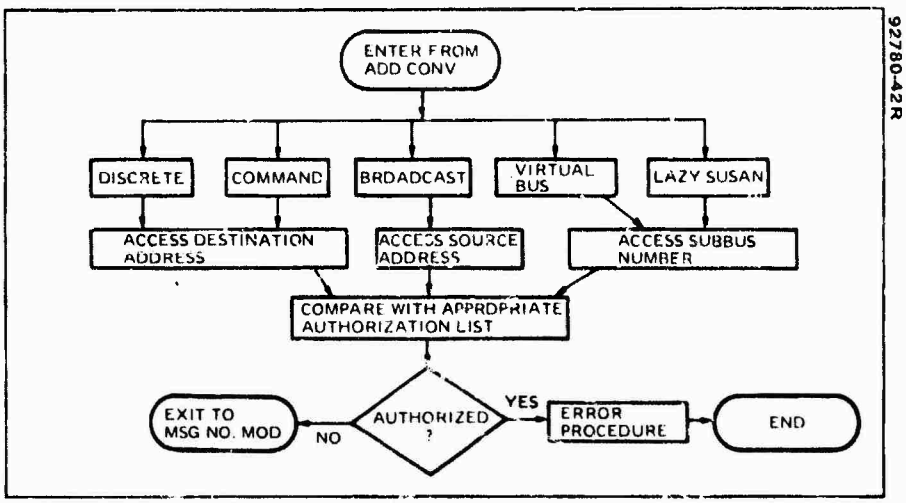


Figure 4.6.B.7-1. Transmit Authorization Check. The transmit authorization check prevents DTEs from establishing links with unauthorized devices.

8. MESSAGE NUMBER MODIFICATION

Each LIU maintains a count of the number of valid messages its associated DTE has sent for each message type. The LIU inserts the current count into each message header.

After the DTE message passes the authorization check, the Local Intraconnect Unit (LIU) performs either three or four modifications to the message header, depending on message type. The four possible modifications are: message number, sequence number, system time, and header error check.

The message number (m) is a count per source per type of message Each LIU maintains a running total of the number of valid messages its associated DTE has sent for each of the five message types. A separate count is maintained for discrete messages, for LIU-directed command messages, for DTE-directed command messages, for local broadcast messages, for external broadcast messages, for messages on each of the sixty three subbuses in the Virtual Bus channel, and for messages on each of the sixty-three subbuses in the Lazy Susan channel (see Figure 4.6.B.8-1).

The LIU increments the appropriate counter by one each time a message is received from the DTE. The LIU then reads the counter and places the contents in the fifth word of the message header. For Lazy Susan messages, the counter is only incremented if the DTE is designated a Lazy Susan source DTE.

The contents of the counters are set and cleared via command messages. The command messages can be originated by the FI Manager, by the LIU's associated DTE, or by another DTE acting as the user group manager. The LIU reports the contents of the counters to the associated DTE and to the FI Manager via command messages.

The message number associated with each message allows a destination DTE to sort messages into source generation order regardless of the arrival times. In addition, the message number associated with each message assists system checkout and monitoring by the user group manager or the FI Manager. The totals in the message number counters can be used to determine which DTEs have the heaviest activity and to monitor FI system traffic loads.

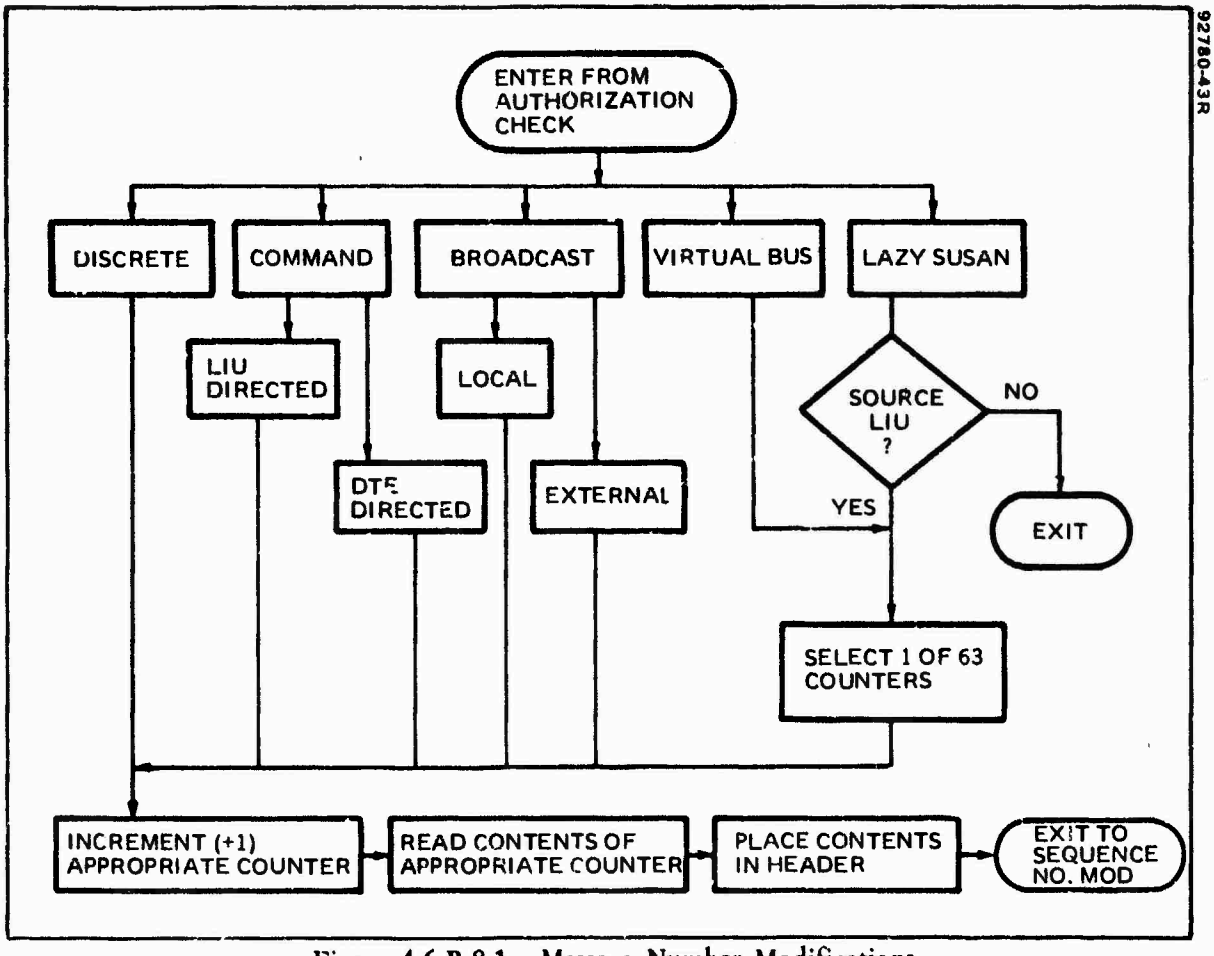


Figure 4.6.B.8-1. Message Number Modifications

9. SEQUENCE NUMBER MODIFICATION

The Sequence Number modification function maintains transmission discipline on subbuses within the Virtual Bus and Lazy Susan channels by preventing contention between users.

When a subbus is established, each time slot in that subbus has a Sequence Number associated with it (see Figure 4.6.B.9-1). The first time slot has Sequence Number one associated with it, the second time slot has Sequence Number two associated with it, etc. The Sequence Number is a modulo 2^{16} or 65,536 count. Each subbus Sequence Number count is independent of other subbus Sequence Number counts. The Sequence Number differs from the message number in that the Sequence Number transcends individual DTEs and governs the order of transmissions on subbuses, whereas the message number is associated with individual DTEs and is independent of the order of transmissions on subbuses (see topic 4.6.B.8). Sequence Number utilization on the Virtual Bus subbuses is slightly different than Sequence Number utilization on the Lazy Susan subbuses.

For Virtual Bus operation, one of the subbus member DTEs or the FI Manager acts as a subbus controller. The controller assigns slot times in which each DTE transmits. This is accomplished by specifying an offset and a radix. A DTE with an offset of 5 and a radix of 10 transmits on sequence numbers 5, 15, 25, 35..., until notified otherwise by the controller. Similarly, a DTE with an offset of 7 and a radix of 10 transmits on Sequence Numbers 7, 17, 27, 37,..., until notified otherwise by the controller. When not transmitting in a time slot, every DTE member of a Virtual Bus (subbus) receives all messages in those time slots.

DTE members of a Virtual Bus (subbus) need not be concerned about transmitting on the appropriate Sequence Numbers. This is a service each LIU of the FI provides to its associated DTE. Via command messages, the subbus controller notifies each LIU of the Sequence Numbers that the DTE is permitted to transmit on. The subbus controller also synchronizes each LIU's Sequence Number counter to the correct value on that subbus. After synchronization, the LIU increments its Sequence Number counter for each subbus with each occurrence of a time slot in that subbus.

After the LIU inserts a message number (m) into a Virtual Bus message, the LIU examines the subbus number (v) in the first word of the message header. The LIU obtains from its memory the next transmit Sequence Number (q) for that particular subbus and inserts it into the sixth word of the message header (see Figure 4.6.B.9-2). (The Virtual Bus message cannot be given a Sequence Number of a time slot which occurs during the time the LIU requires for this message processing.) The LIU is responsible for placing the Virtual Bus message in the subbus time slot which has the same Sequence Number (q) and the same subbus number (v) that appears in the Virtual Bus message header. In this manner, each Virtual Bus subbus is contention free.

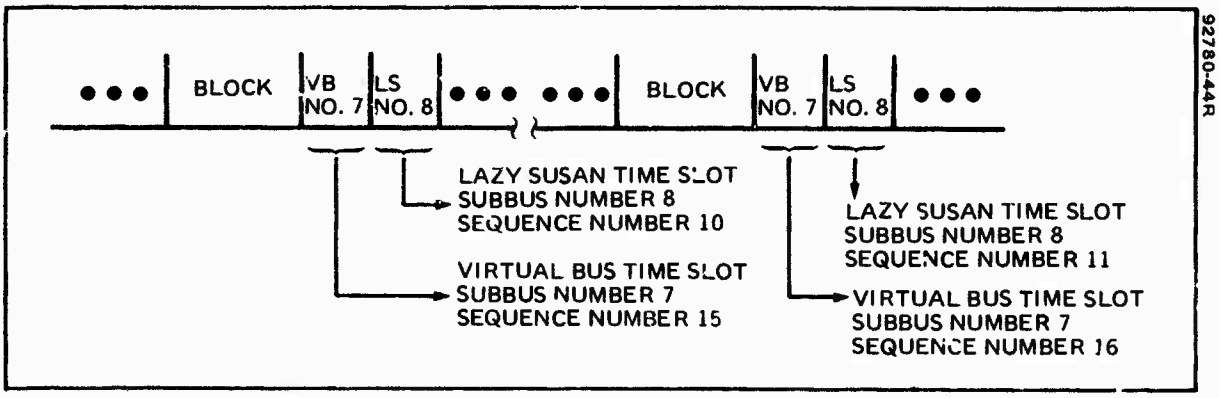


Figure 4.6.B.1-1. Association of Sequence Numbers With Time Slots. Each time slot in a subbus has a Sequence Number associated with it. Each subbus Sequence Number count is independent of other subbus Sequence Number counts since all subbuses are not established simultaneously.

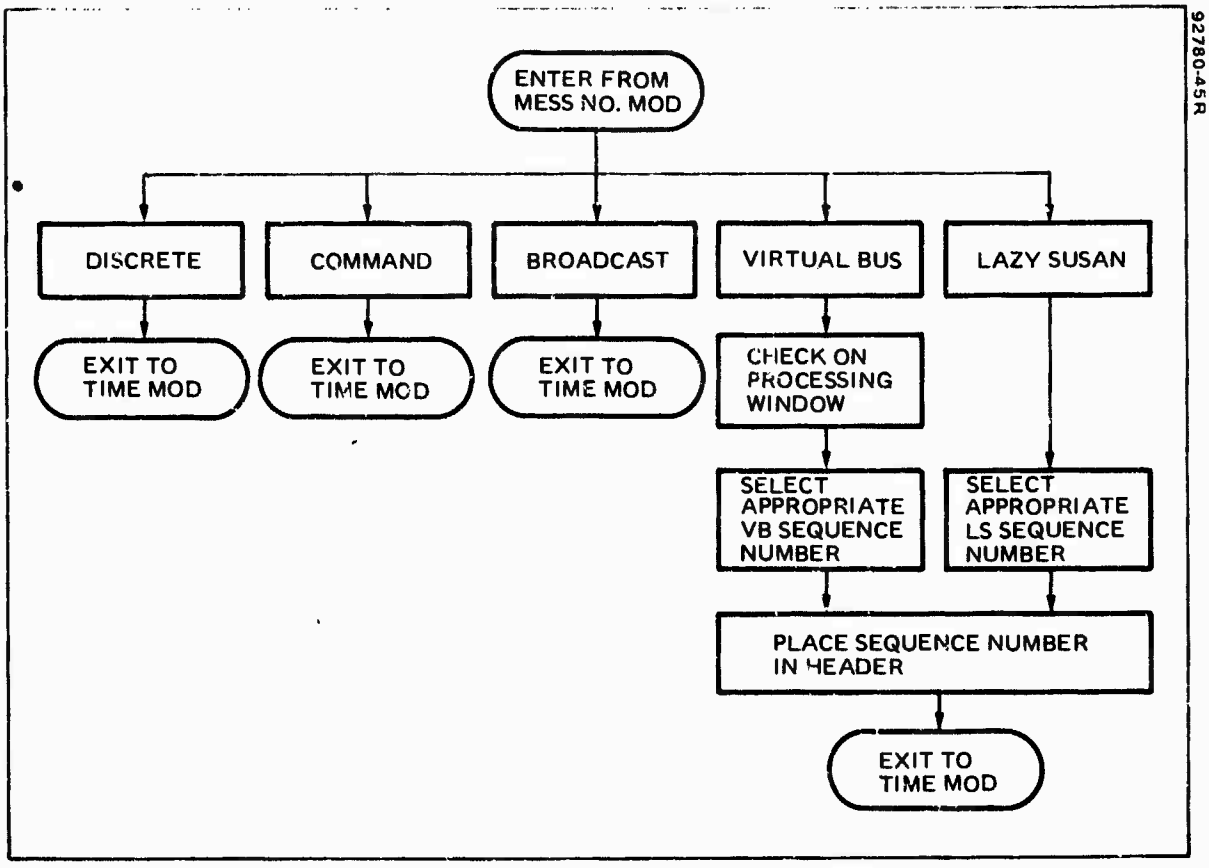


Figure 4.6.B.9-2. Sequence Number Modification. The LIU inserts the appropriate Sequence Number into Virtual Bus and Lazy Susan message headers. The LIU is responsible for placing the messages in the subbus time slot which has the same Sequence Number and the same subbus number that appears in the message header.

For Lazy Susan operation, Sequence Numbers ensure sequential processing of a data field by members of a given subbus. The DTE acting as a Lazy Susan source assigns each time slots for transmit to each member DTE. Again, this is accomplished by specifying an offset and a radix. The source DTE generates a data field which is operated on sequentially by the other members of that particular Lazy Susan subbus. Each DTE member only receives in the time slots which have Sequence Numbers immediately preceding the Sequence Numbers it is permitted to transmit on, assuring sequential processing of one data field.

DTE members of a Lazy Susan subbus need not be concerned about transmitting and receiving on the appropriate Sequence Numbers. The source DTE notifies each member DTE's associated LIU of the Sequence Numbers that the DTE is permitted to transmit on. The source DTE also synchronizes each LIU's Sequence Number counter to the correct value for each subbus. After synchronization, the LIU increments its Sequence Number counter for each subbus for each occurrence of a time slot in that subbus.

After the LIU inserts a message number (m) into a Lazy Susan message, the LIU examines the subbus number (v) in the first word of the message header. The LIU obtains from its memory the Sequence Number immediately after the Sequence Number of the received message and inserts it into the sixth word of the message header (see Figure 4.6.B.9-2). The next Lazy Susan time slot in each subbus cannot occur during the time the LIU requires for this message processing, or the time the DTE requires to operate on the data field. It is the responsibility of the Lazy Susan source DTE when establishing the Lazy Susan subbus to ensure that sufficient processing time occurs between each time slot on the subbus. The LIU is responsible for placing the Lazy Susan message in the subbus time slot which has the same sequence number (q) and the same subbus number (v) that appears in the Lazy Susan message header.

10. TIME MODIFICATION, PARITY RECOMPUTATION, AND MESSAGE SORTING

Three LIU functions – a System Time modification, an error check recomputation, and a message sorting routine – complete the series of checks and modifications performed on a DTE message prior to its transmission on the LI.

Once the LIU completes the sequence number modification on the DTE message, the LIU performs, in the following order, a System Time modification, an error check recomputation, and a message sorting routine.

The System Time function is a historical and an intrusion prevention service provided by the FI to the user. The function consists of a System Time modification executed by the LIU associated with the source DTE and a System Time check executed by the LIU associated with the destination DTE. The source LIU time tags DTE message generation for historical purposes and for use by the destination LIU as an intruder detector. An intruder's retransmission of stale messages can be detected by determining if the elapsed time between message generation and message reception exceeds a permitted time margin.

To accomplish the System Time function, the FI uses a standard time reference based on a universal time date scheme. System Time is measured from midnight of January 1, 1900 and the unit of measure is 1.0 microsecond. System Time is represented by a binary number of 52 digits yielding a time period of 142.7 years. The 16 least significant bits provide time resolution up to 0.066 seconds; the 32 least significant bits provide time resolution up to 1.19 hours. System Time is kept in each shelter of the FI by means of a time crystal, or clock.

A key feature of the FI design is that the transmission timing structure in each shelter is asynchronous with respect to the transmission timing structure in every other shelter. As a result of this feature, the System Time in each shelter is similarly asynchronous with respect to the system times in every other shelter. However, since all the time clocks of the FI are within such close tolerance of each other, the concept of a System Time does have meaning.

Each shelter has only one time clock. It is resident in the Local Intraconnect Control Unit (LICU) and is responsible for maintaining the accuracy of the System Time within each shelter. The LICU continuously supplies one microsecond clock pulses to each LIU via the System Time (ST) line in the Control Bus Interface (CBI). Each LIU increments the 52-bit time counter with each ST pulse.

The system time counter in the LIU is set to the current system time during initialization via command messages and is updated, as needed. The content of the system time counter is reported via command messages. The LIU reports the contents of the System Time counter to its associated DTE by placing a command message in the local portion of the LIU message storage in queue behind other messages already in the local portion. The LIU reports the

contents of the System Time counter to the FI Manager by placing a command message in the block portion of the LIU message storage in queue behind other messages already in the block portion.

To perform the System Time modification function, the LIU first reads the System Time counter and places its contents in the appropriate header word. The LIU inserts: 1) the 4 most significant bits (g) of the System Time into the seventh header word, 2) the 16 lower order bits (h) of the 20 most significant bits (g, h) of the System Time into the eighth header word, 3) the 16 higher order bits (j) of the 32 least significant bits (j, k) of the System Time into the ninth header word and 4) the 16 least significant bits (k) of the System Time into the tenth header word.

After insertion of the System Time into the header of every valid message, the LIU executes the error check recomputation function.

The error check recomputation function is vital to the protection of the System Time information and all other FI provided service information which is inserted into the message header. Since information has been inserted into the message header, the longitudinal parity check word (e) supplied by the DTE in the message header is no longer correct. Therefore, the source LIU performs a longitudinal parity computation on the first fifteen header words and inserts this recomputed check word (e) into the sixteenth header word.

Since the message handling accomplished after input from the DTE results in messages occupying undesignated successive memory locations in the LIU message store, these memory locations must be designated in terms of Block, Virtual Bus, and Lazy Susan. (See Topic 4.6.A.2.) The message sorting function performs this task.

Placement of the five types of DTE messages on to the Local Intraconnect (LI) is performed by three transmission procedures: Block (discrete, command, broadcast messages), Virtual Bus, and Lazy Susan.

Part 4 – Task III, Preliminary Design Analysis
Section 6 – Local Intraconnect Unit Description
Subsection C – LIU to LI Data Transfers

1. OVERVIEW OF TRANSFERS FROM LIU TO LI

The LIU, using three separate transmission procedures to complement the channel structure of the LI, maximizes use of time slots and minimizes contention and bottleneck problems.

Each shelter in the FI system contains a common data distribution bus designated as the Local Intraconnect (LI). The LI is a time division multiple access (TDMA) bus divided into block (Virtual Bus (VB) and Lazy Susan (LS)) channels. The LIU interfaces directly with each piece of DTE and provides each DTE with access to the three channels of the LI. In providing the DTE with access to the LI, the LIU utilizes three separate transmission procedures to efficiently place DTE messages into the proper channel of the LI. (See Figure 4.6.C.1-1).

The LI, and each channel of the LI, is a TDMA structure. Before being divided up into time slots, the VB and LS channels are each first partitioned into 63 sub-buses. Each sub-bus is then divided into time slots. Each sub-bus in the VB and LS channel provides a guaranteed capacity to the user. To achieve this guaranteed capacity, time slots in a sub-bus occur at regular intervals. However, since not all sub-buses are identical, the overall occurrence of sub-bus time slots is irregular. In such a structure, VB and LS time slots have precedence over Block time slots. The Block channel is divided directly into time slots since there is no sub-bus structure.

Different message types are distributed to each of the channels (see Figure 4.6-15) from designated storage areas in the LIU. All three transmission procedures respond to timing and control information supplied to the LIU by the LICU via the Control Bus Interface. The existence of three separate procedures leads to efficient transmission of messages on the LI. Messages can be placed on the LI as the proper time slots become available, regardless of whether or not the order of transmission is equivalent to the generation order of the messages.

The Block transmission procedure consists of a reservation sequence and a transmission sequence. During the reservation sequence, the LIU obtains a time slot assignment from the LICU. In order to do this, the LICU needs to know if an LIU desires slots and how large it must be. The LICU obtains this data by polling each LIU which then responds with a reservation request containing the needed information.

After transferring an "active" reservation to the LICU, the LIU enters the transmission sequence. The LICU assigns a time slot to the LIU based on information in the reservation request and on information from the memory status lines. When the assigned time slot arrives, the LICU polls the LIU. That LIU then places the Block message on the LI. Since the LICU packs Block messages, this polling appears random to the LIUs.

By taking reservations and assigning LIUs to a specific time slot, the LICU prevents contention in the Block channel. By performing a memory status check prior to the time slot assignment, the LICU prevents bottlenecks in the

Block channel. The ability to prevent contention and bottlenecks is a key feature of the FI system.

The mechanics of the VB and LS transmission procedures are identical. Both procedures are based on the use of the sequence number in the message header. The procedures are slightly different because the sequence numbers have different implications in each channel. However, in both channels, the sequence numbers prevent contention and bottlenecks.

When a subbus is established, each time slot in that subbus has a sequence number associated with it. Since subbuses are established gradually as the system operates, each subbus sequence number count is independent of other subbus sequence number counts. When a DTE communicates on a subbus, the DTE is assigned certain time slots – by specifying sequence number – in that subbus in which is to transmit the assigned sequence numbers are stored in the LIU.

As stated previously, the LIU inserts one of the assigned sequence numbers into the VB and LS message headers during the sequence number modification. The transmission function procedures for each channel examine the message header and place the message in the time slot which has the same subbus number and same sequence number that appear in the message header. Timing information from the LICU notifies the LIU of subbus time slot boundaries. In addition to maintaining this transmission discipline in the VB and LS channels, the sequence numbers also ensure sequential processing of data in the LS channel.

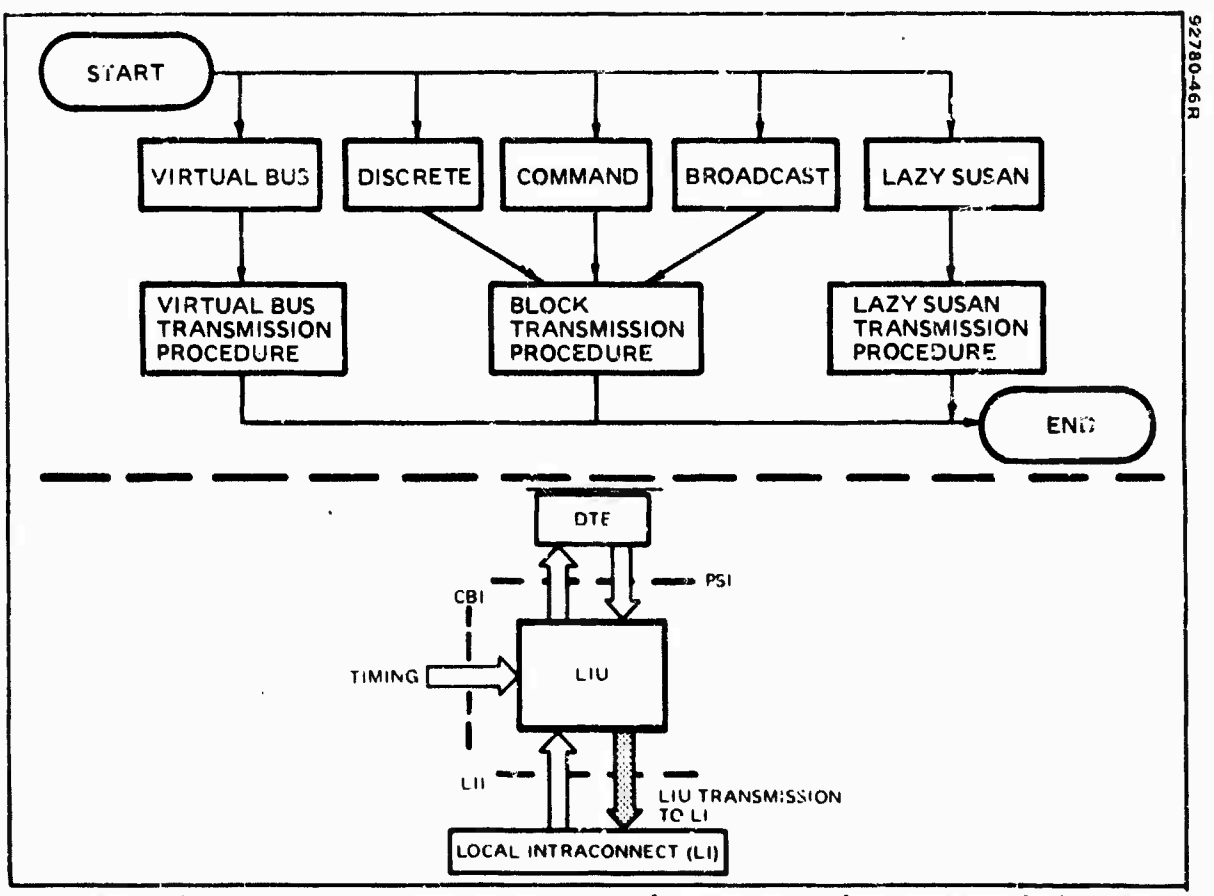


Figure 4.6.C.1-1. LIU Transmission to LI. Utilizing timing information supplied by the LICU, the LIU selects the appropriate procedure and places messages on the LI.

2. BLOCK MESSAGE TRANSMISSION

Block message transmissions are synchronized with assigned time slots under control of the LICU.

The Block message transmission process consists of a reservation sequence and a transmission sequence.

Reservation Sequence – In order to transmit a Block message on the LI, the LIU must obtain a time slot assignment from the LICU. This is accomplished by a poll-response sequence during which the LIU informs the LICU of its need for time slots, their size, and the type of message. The LIU response to the poll is called a reservation request.

The LICU requires six pieces of information from the LIU: 1) The LICU must know if a time slot is in fact desired. When occupied, the Block portion of the LIU message storage contains messages which are in queue and waiting to be transmitted. 2) Assuming there is a Block message, the LICU must know if the message is point-to-point or broadcast since the latter does not require a memory status check. 3) If the message is point-to-point the LICU must know whether the message is for local transmission or external transmission since the memory status check performed for local transmission is different from that for external transmission. 4) The LICU must know the destination EIU address for external messages and the destination LIU address for local messages. This data is needed since the LICU checks the status of the memory in the destination before enabling the source LIU transmission. 5) The LICU must know the source LIU address so that it knows which LIU is making the request and can enable the proper LIU for transmission at the appropriate time. 6) Since Block message lengths are variable and since the LICU packs messages into the Block channel in order to obtain maximum utilization of the channel, it needs to know message length. Based on the six items of information, reservation requests are either one 18-bit or two 18-bit words long.

The information needed to construct a reservation request is copied when possible and derived only when necessary. Message headers are the source of copied information. The LIU accesses various parts of the header section and assembles the information into a reservation request (see Figure 4.6.C.2-1). To keep the LIU processing to a minimum, the same number of information bits are specified in the reservation request as in the message header when conveying the same information. Thus, the LIU directly copies the source LIU address (z), the destination EIU address (w), and the destination LIU address (x) into the appropriate fields of the reservation request structure. The reservation request structure is described below.

The first reservation request word has the following format:

ψ ξξξ ξξξξ u uuzz zzzz

The reservation flag (ψ) is a 1-bit field. The reservation flag is asserted when a time slot is desired. The message flag (γ) is a 1-bit field. The message flag is asserted for multiple destination messages. The destination address (ξ) is a 7-bit field. The most significant bit (ξ_6) is asserted for external transmission. The six least significant bits ($\xi_5 - \xi_0$) then contain the EIU destination address (w). The most significant bit (ξ_6) is negated for local transmission. The six least significant bits ($\xi_5 - \xi_0$) then contain the LIU destination address (x). The LIU source address (z) is a 6-bit field. The 3 bits in the first reservation request word are unused (u) and set to logical zero.

The second reservation request word has the following format:

u uuuu uλλλ λ λλλλ λλλλ

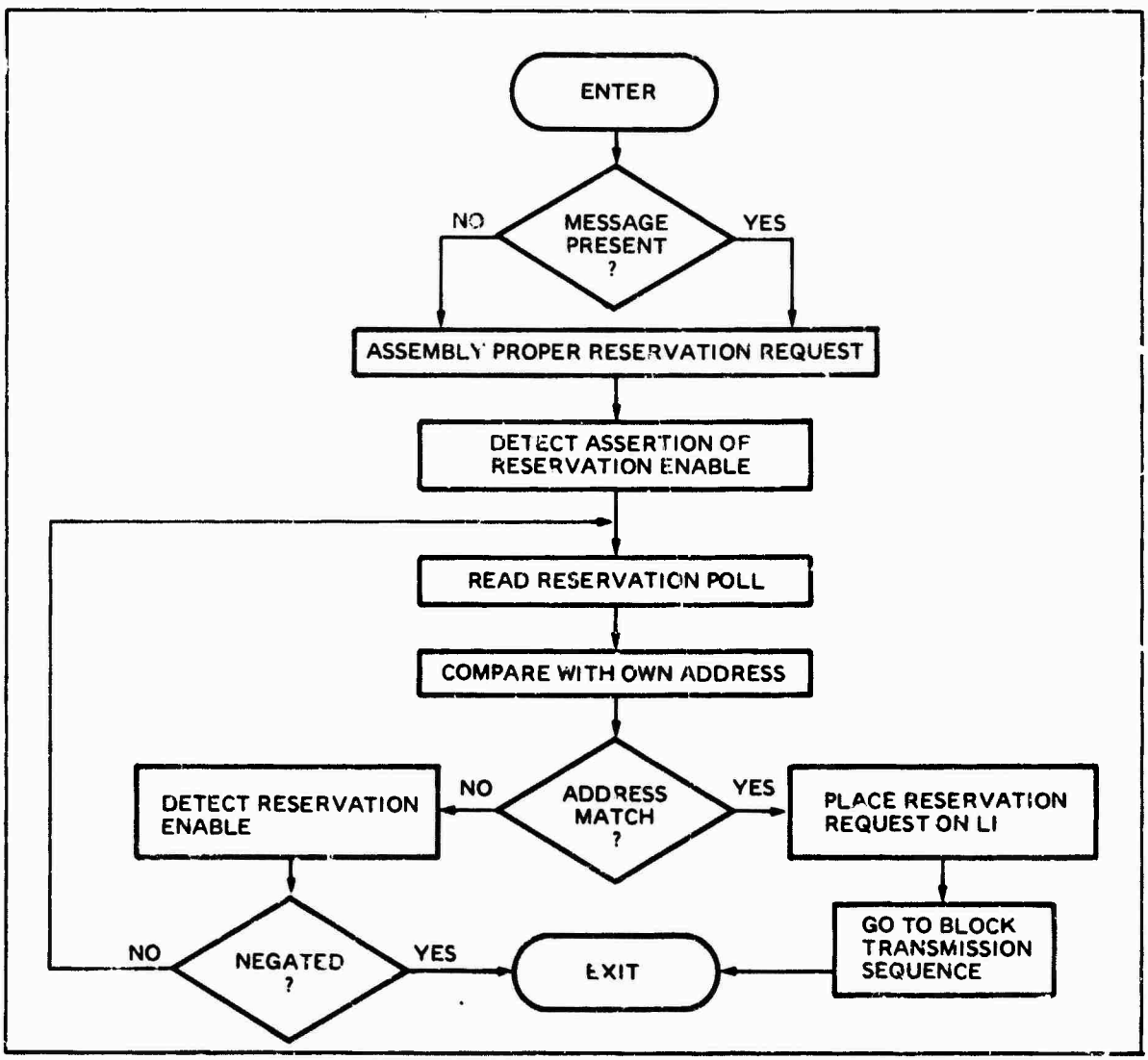


Figure 4.6.C.2-1. Block Reservation Sequence. The reservation request contains the information the LICU requires to assign a LIU a time slot. The LIU transfers a reservation request when polled by the LICU.

2. BLOCK MESSAGE TRANSMISSION (Continued)

The message total word count (λ) is a 12-bit field. The LIU biases the data section word count (c) by 16 to determine the overall message length. (Every header section contains 16 words.) The 6 bits of the second reservation request word are unused (u) and set to logical zero. If the reservation flag (ψ) is negated, the second reservation request word is neither generated by the LIU nor transferred by the LIU to the LICU.

During reservation periods, reservation polls and reservation requests are exchanged between the LICU and LIUs. These exchanges are made via the LI. The LICU initiates a reservation period by asserting the Reservation Enable line in the Control Bus Interface (CBI). The LICU transmits a one word reservation poll containing a specific LIU address to all LIUs. Each LIU correlates the address in the reservation poll with their own unique address. The LIU whose address matches that of the poll then transmits a reservation request back to the LICU. Reservation polls and reservation requests are exchanged at the LI data rate of 96 Mb/s.

Transmission Sequence – After the LIU has transferred the reservation request to the LICU, the LIU places the message length (λ) in the word counter (see figure). The word counter is decremented for each word placed on the LI. Since transmission may be temporarily suspended by insertion of VB and LS operations, the LIU uses the contents of the word counter, rather than a time period to determine the end of message transfer.

The LICU initiates a transmission period by asserting the Transmission Enable line in the CBI and transmitting a one word transmission poll to all LIUs. The transmission poll contains the address of the LIU which has been assigned the time slot. Only the LIU whose address correlates transmits during the transmission period.

The LIU, which is assigned to the time slot in a given transmission period, places one word of its message each time the LICU provides a Data on Bus (DOB) pulse. After each word, the LIU decrements the word counter by one (see figure). Before placing the next message word on the LI, the LIU checks the VB/LS lines in the control bus interface to determine if a VB or LS operation is required. The occurrence of a sub-bus time slot suspends a Block message transmission until the completion of that sub-bus time slot. The Transmission Enable line remains asserted during these pauses, thereby indicating the continuation of the same Block message after the pause.

After any such pauses, the LIU once again places block message words onto the LI and continues to do so until the word counter reads zero. The Transmission Enable remains asserted for a brief period after the end of each Block message to allow the destination LIU to perform the LII receive transfer error check (see Topic 4.6.D.4. As part of the LII receive transfer error check, the destination LIU sends an ACK/NACK to the source LIU After the source LIU has received the ACK/NACK, the LICU negates Transmission Enable.

Upon receiving the ACK/NACK, the source LIU performs one of two separate routines. If the destination LIU sent an ACK, the message was received

without errors and the source LIU erases the message from the Block portion of its message store. The source LIU then assembles a reservation request for the next message in queue in the Block portion.

If the destination LIU sent a NACK, the message was received with errors the source LIU reassembles a reservation request for the same message and repeats the entire Block transmission procedure. The second message in queue in the Block portion of the LIU message storage must wait until this first message in the queue is transferred to a destination LIU without errors.

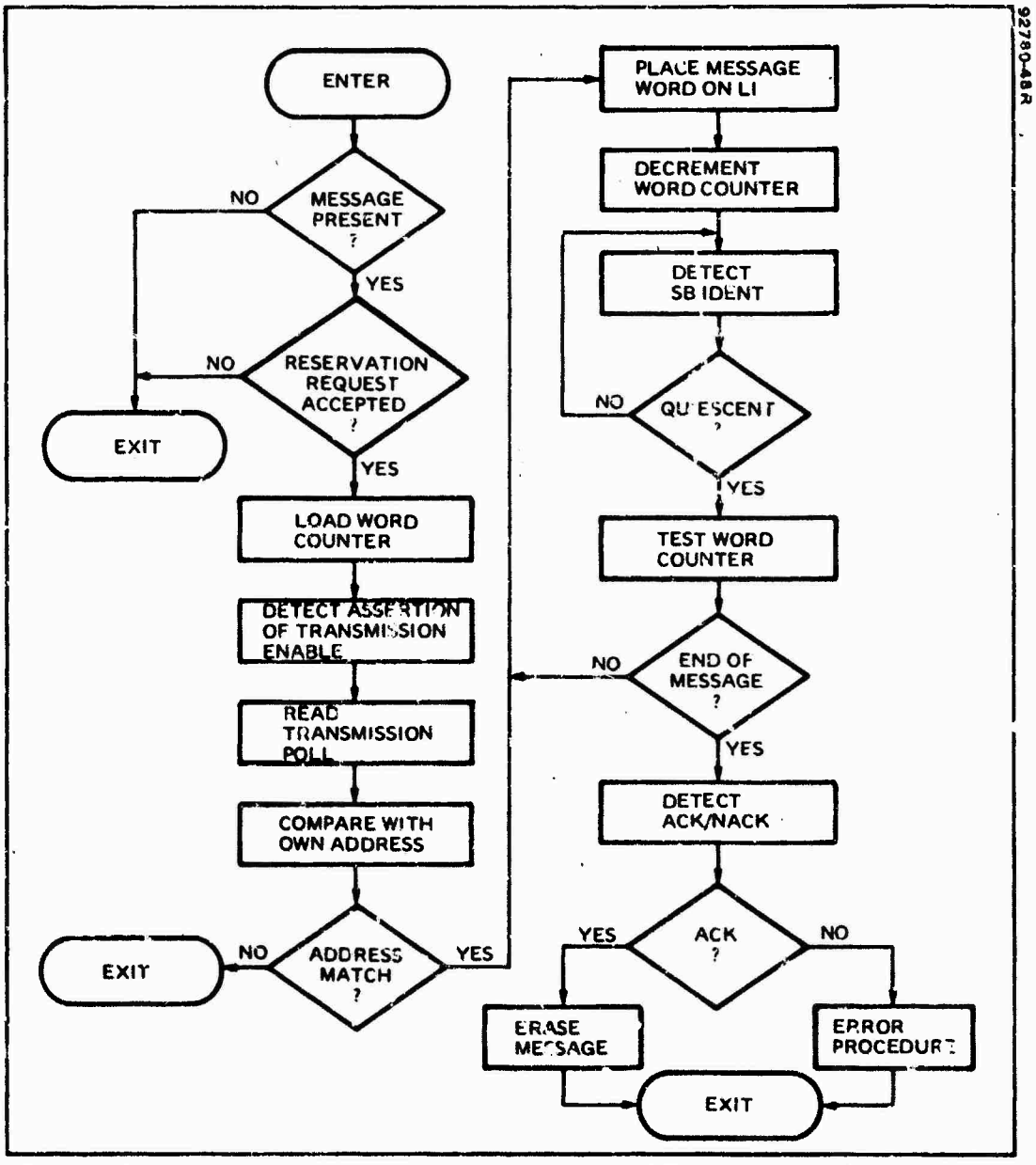


Figure 4.6.C.2-2. Block Transmission Sequence. The LIU transmits a block message when polled by the LICU. The LIU's transmission may be temporarily suspended by the occurrence of a time slot in a virtual bus or lazy susan subbus.

3. VIRTUAL BUS AND LAZY SUSAN TRANSMISSIONS

The mechanics of the Virtual Bus and Lazy Susan transmission processes are nearly identical. Only the procedures for the sequence number modification are different.

The VB and LS messages are distributed in the VB and LS channels, respectively, of the LI. Placement of these two types of messages on the LI is handled by two transmission processes whose mechanics are nearly identical.

To review, the LI (therefore each channel in the LI) is a time division multiple access (TDMA) structure. Before being divided up into time slots, the VB and LS channels are each first partitioned into 63 subbuses. Each subbus is then divided into time slots and each time slot has a Sequence Number associated with it. The Sequence Number is a modulo 2^{16} count. Each subbus Sequence Number count is independent of the other subbus Sequence Number counts.

Each subbus has a group of DTEs assigned to it; either the DTE which is the VB subbus controller, or the DTE which is the LS subbus source, or the FI system manager assigns time slots to each DTE member of a subbus; the member DTEs may only transmit messages in assigned time slots. The time slots are assigned by specifying the Sequence Numbers which are stored in each member DTE's associated LIU. During Sequence Number modification, the LIU inserts one of the assigned Sequence Numbers into VB and LS message headers.

The VB and LS transmission processes are dependent on subbuses and sequence numbers. The LIU monitors the VB/LS lines in the Control Bus Interface (CBI) since transistions to stable logic levels notify the LIU of VB and LS time slot boundaries. (The VB/LS control lines are in the quiescent state during the Block channel.) The LIU also maintains a Sequence Number counter for the subbuses of interest to the LIU's associated DTE.

Since the mechanics of the two processes are identical, the VB case is discussed below with the LS case in parentheses.

The VB (LS) portion of the LIU message storage contains VB (LS) messages which are in queue and waiting to be transmitted in the VB (LS) channel of the LI. When the VB (LS) portion contains a message, the VB (LS) transmission procedure places this message on the LI at the appropriate time. For the first step in the transmission procedure, the LIU accesses the subbus number (v) and the sequence number (q) in the header of the first message in the queue (see figure). The LIU then monitors both the VB/LS control lines and its own Sequence Number counter for that subbus number (v). The LIU transmits a VB (LS) message in a time slot in the LI when the binary representation on the VB/LS control lines matches the subbus number (v) and when the Sequence Number counter matches the Sequence Number (q).

The LIU continues to place message words on the LI until the VB/LS control lines change. When they change, the binary representation no longer matches the subbus number (v) in the message header. Since, in establishing the subbus the VB subbus controller (LS subbus source) establishes time slots which were of sufficient size for the length of messages generated by the DTE

members, the entire message will have been sent. The VB (LS) transmission procedure is then repeated for the next message in queue in the VB (LS) portion of the LIU message store.

Unlike block transfers, the LIU does not retain copies of messages until an acknowledge is received from the destination LIU. Retransmission of VB and LS messages is the responsibility of the source DTE. (An LIU retransmission of an LS message destroys the proper sequential processing of a data field.)

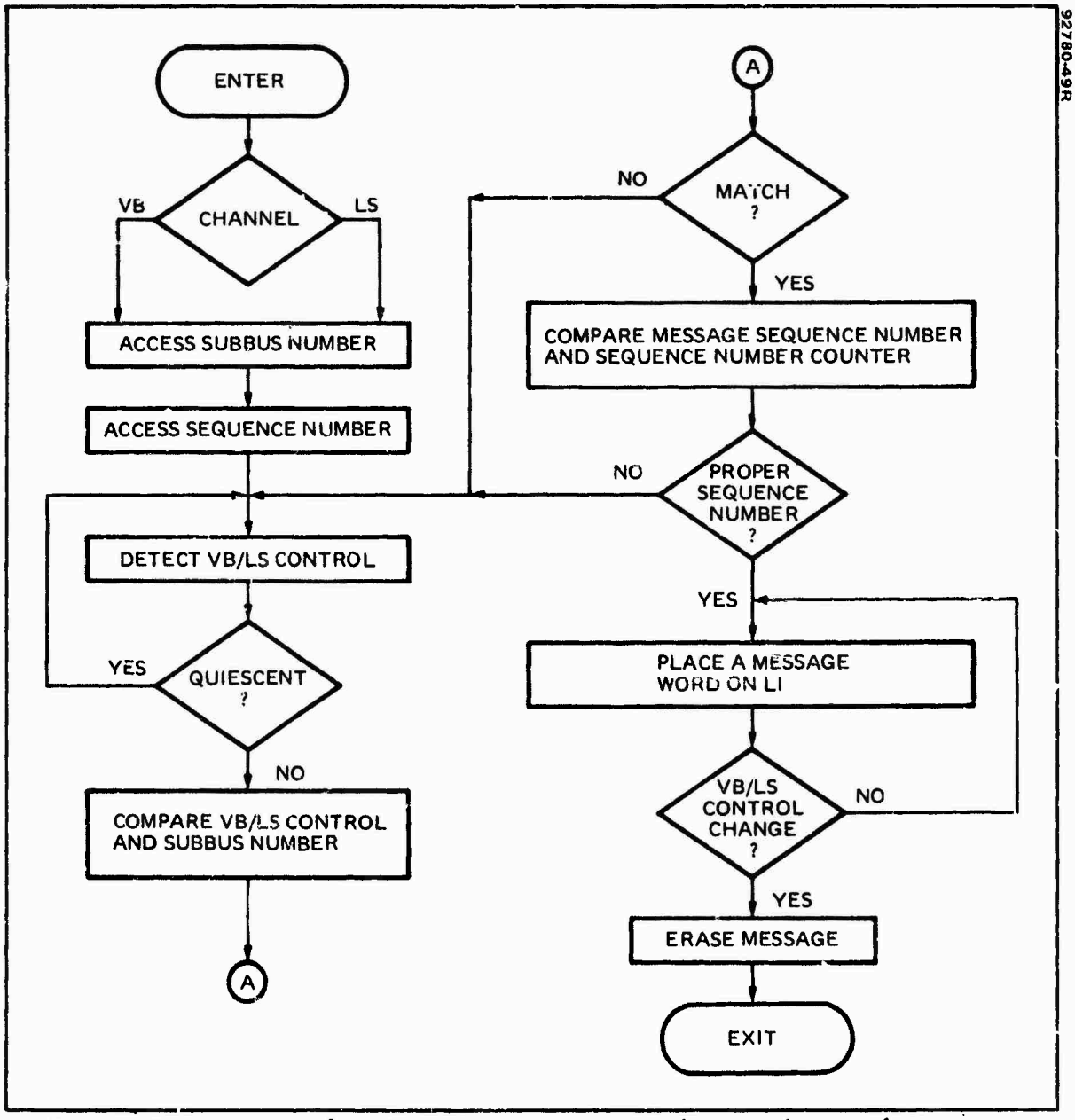


Figure 4.6.C.3-1. VB and LS Transmission Process. In the Virtual Bus and Lazy Susan Channels, the LIU places the corresponding message in the time slot which has the same subbus number and the same sequence number that appears in the message header.

1. OVERVIEW OF TRANSFERS FROM LI TO LIU

The LIU uses three separate reception processes in accepting messages from the LI. It also performs checks to ensure that transfers from the LI were correct.

Reception of messages from the LI involves a sequence of message reception, message checks, and message modifications (see Figure 4.6.D.1-1). Three reception processes – Block, VB, and LS – handle acceptance of the respective messages types from the LI. All three reception processes respond to timing and control information supplied to the LIU by the LICU via the CBI. The message checks ensure the validity of the message; the message modifications prepare the message for transfer from the LIU to its associated DTE.

For Block message reception, the LICU initiates message reception in the LIU and notifies the LIU when reception is suspended. As in the LIU to LI transfer, Block message transfer from the LI to the LIU may be temporarily suspended by the occurrence of a time slot for a VB or LS subbus. All LIUs continue reception pending the outcome of a destination check. If this check is negative, the LIU halts message reception. If the check is positive, the entire message is stored in either the local or external portion of the LIU message store, depending on the message source.

For VB and LS message reception, the LICU notifies the LIU of subbus time slot boundaries. The LIU selects messages from those particular subbuses of interest to its associated DTE and stores them in the VB/LS portion of its message store. The LIU selects every VB message in a particular subbus of interest, excluding those messages that it transmitted. The LIU selects those LS messages whose Sequence Number immediately preceeds the Sequence Numbers that the LIU is assigned to transmit on, thus ensuring sequential processing of a data field.

The transfer error check consists of a header parity check which has a stringent acceptance threshold and a data parity check which has a predetermined, but variable threshold.

The message type determination verifies the message type code in the message header and sets message processing flags in the LIU. The authorization check determines if the LIU's associated DTE is authorized to receive a particular message.

The address conversion function translates source and destination addresses in the message header from the FI's addressing scheme to the DTE's addressing scheme. The System Time check is an intrusion detection service provided by the FI to the user which prevents stale and invalid messages from disrupting normal operations.

Upon completion of this series of events, the message received from the LI is certified as valid and is ready for transfer to the DTE.

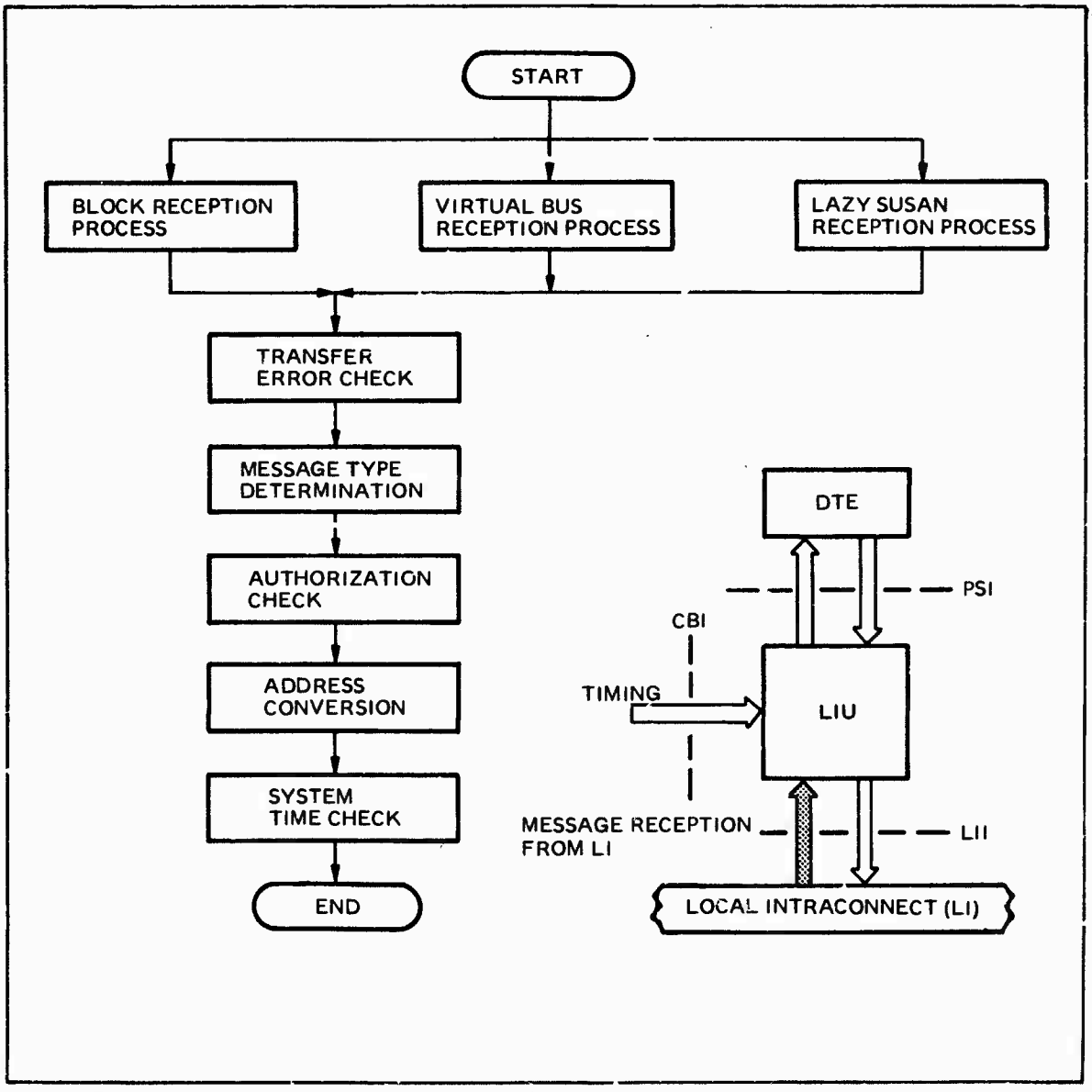


Figure 4.6.D.1-1. LIU Reception From LI. The LIU performs the necessary validation checks to ensure proper transfer to its associated DTE.

2. BLOCK MESSAGE RECEPTION PROCESS

Message acceptance/rejection decisions are rapidly performed since the first four words of the header contain all the information related to message reception needed by the LIU.

Block messages are removed from the Block channel of the LI by the Block reception process (see figure) and are stored in either the local or the external portions of the LIU message store. The Block reception procedure responds to control signals supplied to the LIU by the LICU via the CBI. The Block reception process is the inverse of the Block transmission sequence used to transfer messages to the LI from the LIU.

The LICU must notify every LIU when reception of a Block message starts and when reception is suspended since VB and LS channels may interrupt Block message transmission. Notification of the starting point is required since the beginning of a Block message is not always coincident with the beginning of a Block transmission. This Block message arrangement contrasts with the VB and LS message arrangement in which VB and LS messages always start at the beginning of their respective channels.

The LICU initiates a transmission and reception period by asserting the Transmission Enable line in the CBI. It then transmits a one word transmission poll to all LIUs. Each LIU correlates the address in the transmission poll with its own address (see Figure 4.6-20). Those LIUs whose addresses did not match begin reception procedures; the LIU whose address did match transmits.

Each LIU uses word pulses to gate message words from the LI. After the removal of each word from the LI, each LIU checks the VB/LS control line to determine its state. Message reception is temporarily suspended if the VB/LS control lines are no longer in the quiescent state. The Transmission Enable line remains asserted during these pauses, thereby indicating the continuation of the same Block message subsequent to the pause. After the pause, the LIU once again uses word pulses to remove message words from the LI.

The destination check is a parallel check on the destination addresses (w, x) and the message type code (t) (since discrete, command, and broadcast messages are all distributed in the Block channel of the LI). For discrete and command messages, the LIU correlates the destination address (w, x) in the second word of the message header with its own unique address. For broadcast messages, the LIU correlates the message type code (t) in the first word of the message header with the valid message type code for broadcast messages. If either correlation yields a match, the LIU reads the entire Block message into that portion of its message store dictated by the source check. If neither correlation yields a match, the LIU halts reception, erases that part of the message already read in, and waits for the next assertion of Transmission Enable. The source check is a check on the source address (y) in the third word of the message header. The LIU places a block message from an LIU within the same

shelter into the local portion of its message store; it places a Block message from an LIU in a different shelter into the external portion of its message store. With this arrangement, extensive local Block message reception activity does not prevent an LIU from receiving external Block messages.

With each message word loaded, the LIU increments the word count and compares the total with the overall message length. To determine the overall message length, the LIU adds 16 to the data section word count (c) in the fourth word of the message header. The entire message has been received when the contents in word count equals the overall message length. After receipt of the entire message, theLIU performs a transfer error check. Based on the outcome of this check, the destination LIU sends to the source LIU an ACK or a NACK. The reception period is complete when the source LIU receives the ACK/NACK and the LICU negates the Transmission Enable.

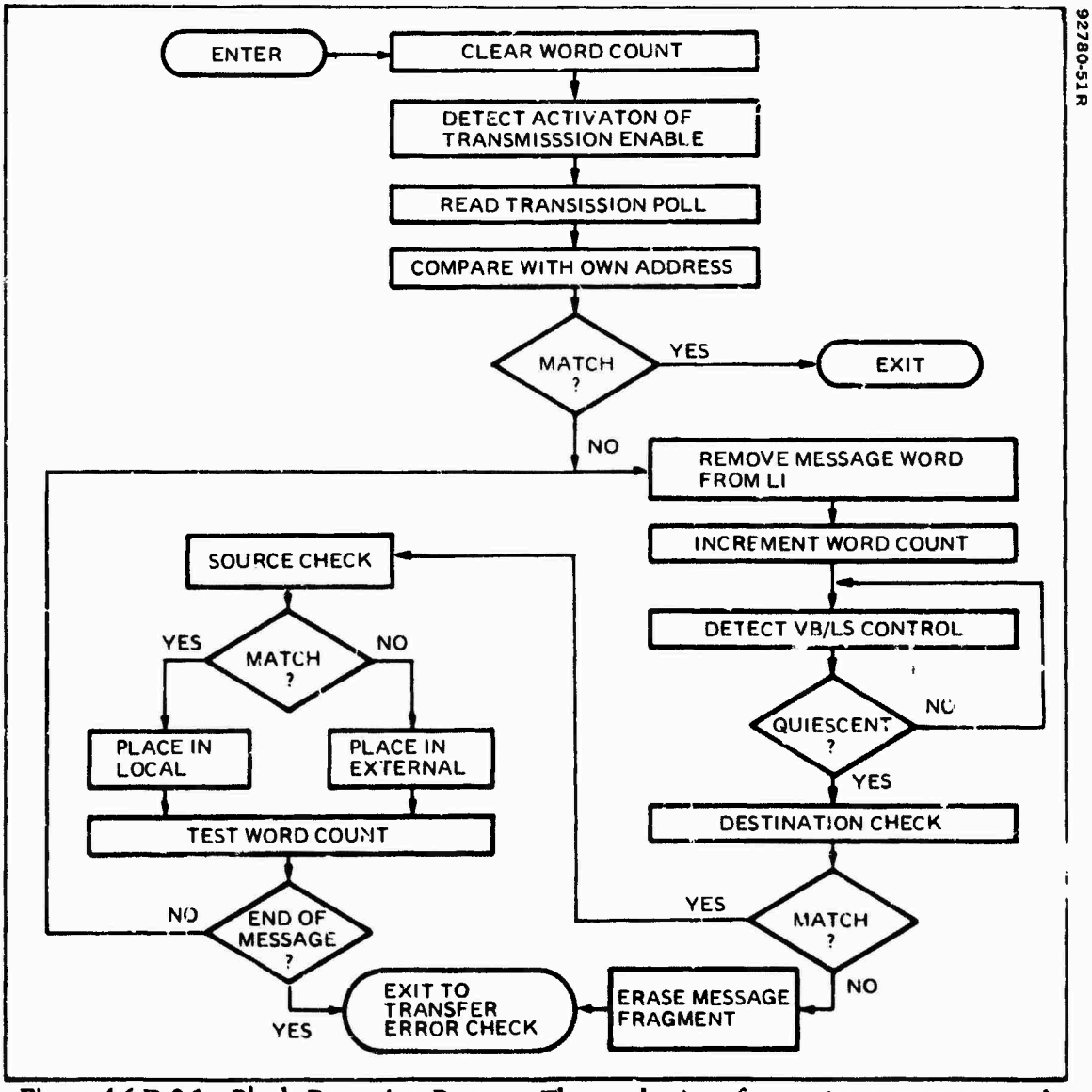


Figure 4.6.D.2-1. Block Reception Process. The mechanics of removing a message word from the LI are the inverse of the mechanics of placing a message word on the LI.

3. VIRTUAL BUS AND LAZY SUSAN RECEPTION PROCESSES

The LIU accepts only those VB and LS messages which are received on a predetermined (programmable) set of subbusses.

The VB and LS messages are accepted from their respective LI channels by separate processes and stored in the VB/LS portion of the LIU message store. The VB and LS reception processes respond to timing information supplied to the LIU by the LICU via the CBI. The mechanics of the two processes are identical.

The VB and LS reception processes are dependent on subbus and Sequence Numbers. The LIU monitors the VB/LS control lines of the CBI since transitions to stable logic levels notify the LIU of VB and LB time slot boundaries. The LIU maintains a Sequence Number (SN) counter for the subbuses which are of interest to its associated DTE.

An LIU receives every VB message in a particular subbus of interest (excluding those messages that the LIU transmitted itself). That is, the LIU removes VB messages from a time slot in the LI when the binary representation on the VB/LS control lines match a subbus of interest and when the Sequence Number counter does not match any Sequence Number on which the LIU is assigned to transmit. (See Figure 4.6.D.3-1.)

An LIU receives selected LS messages in a particular subbus of interest. The LIU removes a LS message from a time slot in the LI when the binary representation on the VB/LS control lines match a subbus of interest and when the Sequence Number counter immediately precedes any Sequence Number on which the LIU is assigned to transmit. In this manner sequential processing of a data field in a message on a particular subbus is guaranteed.

The LIU uses word pulses from the LICU to remove each VB and LS message word from the LI. The LIU continues removing the message words until the VB/LS control lines indicate the end of the time slot by changing to new logic levels (see Figure 4.6-21). The LIU does not maintain a word count to determine when the entire VB or LS message has been received. It is required that, in establishing the subbus, the VB subbus controller or LS subbus source establish time slots which are the proper size for the length of messages generated by the DTE members of that subbus.

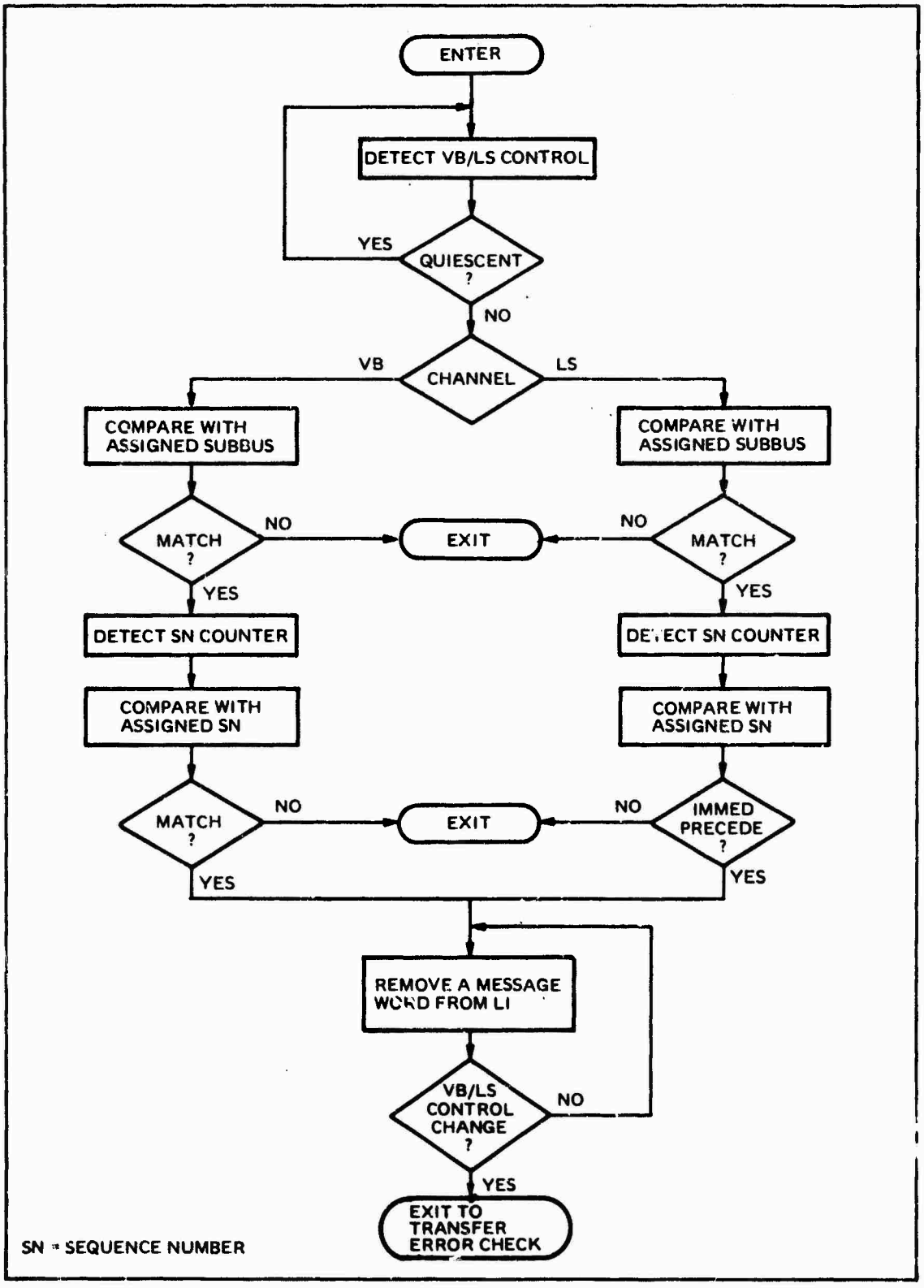


Figure 4.6.D.3-1. The VB and LS Reception Procedure. The mechanics of message removal from the LI are identical for Virtual Bus and Lazy Susan messages.

4. RECEIVE ERROR CHECK

The header error check has a stringent acceptance threshold while the data error check has a predetermined, but variable acceptance threshold. The header error check assures the accuracy of the FI related control information.

Once the LIU has removed an entire message from the LI, the LIU executes a series of checks on the received message. The first check is the Receive Error Check.

After receiving a Block message, the LIU performs a longitudinal parity check on both the header and data sections of the message. If the messages pass the parity check, the LIU immediately sends the source LIU an ACK (see figure. If the message does not pass the parity check, the LIU sends an immediate NACK to the source LIU and generates a command error message addressed to the FI manager. The command error message states that there was a reception error on the LI. The LIU then erases the erroneous Block message.

After receiving a VB or LS message, the LIU performs the same longitudinal parity check as above. However, the LIU does not send an ACK/NACK. The LIU simply initiates an error procedure if the message does not pass the parity check.

During the error procedure, the LIU (1) generates an error command message addressed to the source DTE which notifies the source DTE of the error message, (2) generates an error command message addressed to the FI manager which reports the received message did not pass the parity check, and (3) erases the erroneous Virtual Bus or Lazy Susan message.

Implementation of a rapid ACK/NACK during the error check for block messages maximizes Block message throughput. When the source LIU receives an ACK it erases the message just transmitted from the Block portion of its message storage and prepares to transmit the next message in the queue. This turn-around time is much less than would be required if the ACK was contained in a separate Block message of its own.

In the error procedure for VB and LS messages, it is critical that the LIU addresses a command error message to the source DTE rather than to the source LIU since a source LIU retransmission of a LS message could destroy the proper sequential processing of the data field in the LS message.

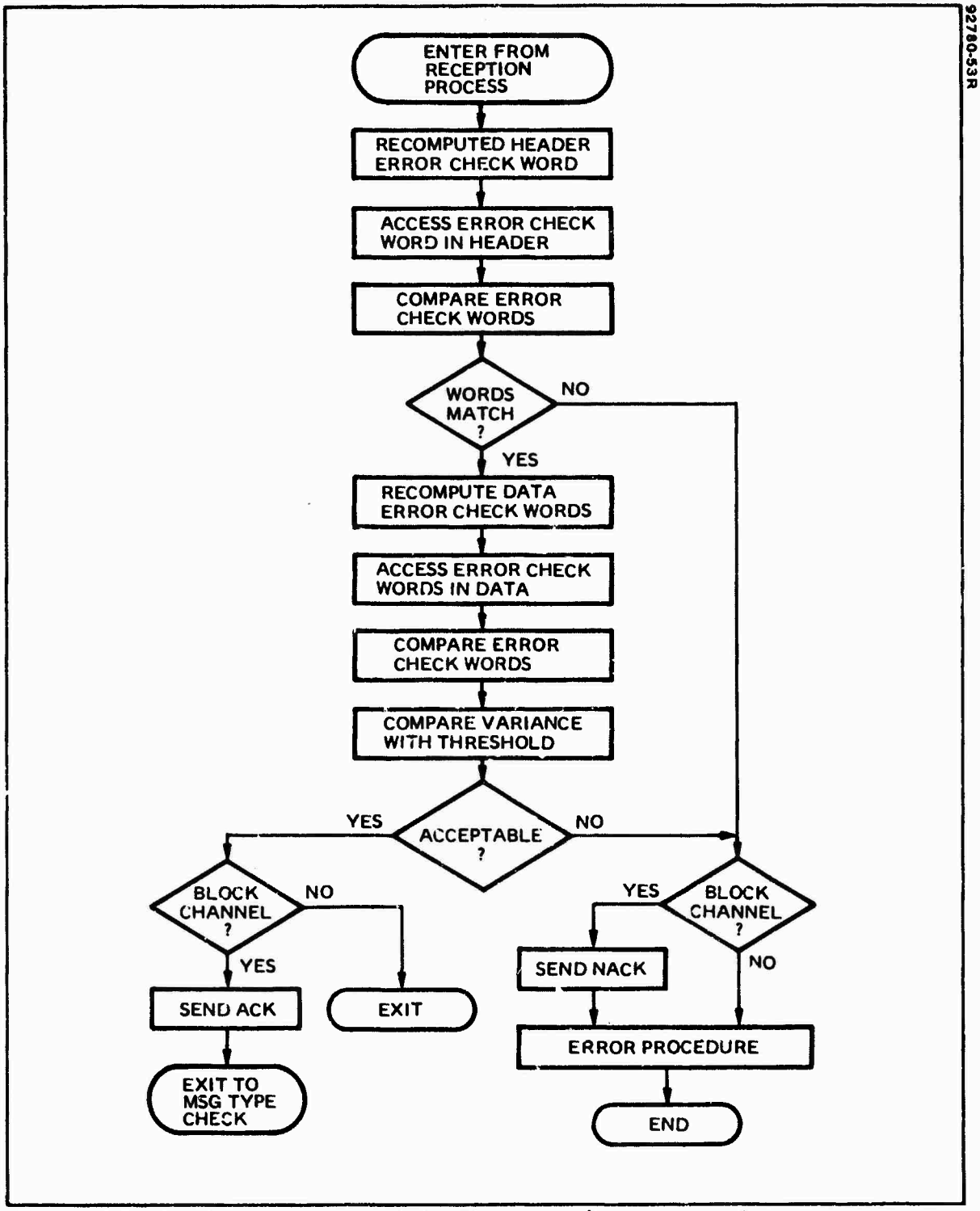


Figure 4.6.D.4-1. The Receive Error Check. The LIU performs an error check on both the data. and header, notifies FI manager of errors, and maintains a source accountability of all errors.

5. ADDITIONAL MESSAGE CHECKS

The LIU performs two validity checks and an address conversion on messages received from the LI.

The LIU determines message type, checks message authorization, and performs an address conversion in preparing a message for transfer to the DTE. The characteristics of these message processing functions are shown in Table 4.6.D.5-1.

In performing the message type determination, the LIU correlates the message type code in the first word of the received message header with its own list of valid message type codes. If the correlation is successful, the LIU sets the appropriate message processing flags. This correlation process is the same as the correlation process in the transmit message type determination. The distinction between the two message type determinations lies in the corresponding error procedures.

During the error procedure for the receive message type determination, the LIU (1) generates an error command message addressed to the source DTE which notifies the source DTE that it must retransmit its message (2) generates an error command message addressed to the FI Manager which reports an invalid message type code in the received message, and (3) erases the erroneous received message.

The receive authorization check is the counterpart of the transmit authorization check and prevents a DTE from gaining access to unauthorized information. The check is based on authorization tables stored in the LIU. For discrete, command, and broadcast messages, the LIU correlates the source address (y, z) in the third word of the message header with its list of authorized source addresses. For VB and LS messages, the LIU correlates the subbus number (v) in the first word of the message header with its list of authorized subbus numbers. If the LIU finds a match during the correlation process, the LIU's associated DTE is authorized to receive that message. If the LIU does not find a match, the DTE is unauthorized to receive that message and the LIU initiates an error procedure.

During the error procedure for the receive authorization check, the LIU (1) generates an error command message addressed to the source DTE that it must request a change in the recipients authorized environment, (2) generates an error command message addressed to the FI Manager which reports an attempted use at an unauthorized environment, and (3) erases the erroneous received message.

The receive address conversion allows each user group of the FI to use its own device addressing scheme independent of the FI addressing scheme. The receive address conversion is the inverse of and similar to the transmit address conversion. The distinction between the two lies in the corresponding error procedures.

During the error procedure for the receive address conversion, the LIU, (1) generates an error command message addressed to the LIU's associated DTE which notifies the DTE that either the DTE must obtain for its LIU all necessary virtual/real address pairs or the DTE must accept real addresses, (2) generates an error command message addressed to the FI Manager which reports that the LIU does not have the virtual address counterpart for a particular virtual address, and (3) erases the erroneous received message.

TABLE 4.6.D.5-1. MESSAGE CHECK CHARACTERISTICS

RECEIVE MESSAGE TYPE CHECK
- similar to transmit message type check
- determines type of message
- correlation process identical
- error procedure different

RECEIVE AUTHORIZATION CHECK
- counterpart of transmit authorization check
- restricts DTE access to information
- correlation process similar
- error procedure different

RECEIVE ADDRESS CONVERSION
- inverse of transmit address conversion
- converts real to virtual address
- error procedure different

6. SYSTEM TIME CHECK

The System Time check function prevents an intruder from rebroadcasting messages in order to spoof the operations of the FI.

The System Time check function is an intrusion prevention service provided by the FI. In performing the System Time check, the LIU accesses the System Time (g, h, j, k) in the seventh through tenth words of the message header. The LIU then adds a pre-established maximum elapsed time (Δt) between message generation by a source DTE and message reception by a destination DTE to the System Time (t_0) in the message header (see figure). The LIU compares the sum of t_0 and Δt with the current System Time, t_1, in the LIU's time counter. If the sum exceeds the current time, that is if $t_0 + \Delta t > t_1$, the message was received within the permitted time margin. If the current time exceeds the sum, that is, if $t_1 \geq t_0 + \Delta t$, the LIU initiates a warning procedure.

During the warning procedure for System Time check, the LIU (1) generates a warning command message addressed to the LIU's associated DTE which notifies the DTE that the following message is potentially invalid, and (2) generates a warning command message addressed to the FI Manager which reports that a message was received after the allocated time interval.

The pre-established value of Δt incorporates several elements. These elements are the variance between the System Time clocks in each shelter, the message processing times required by the source and destination LIU's and the transmission delay times associated with normal FI operation. The value of Δt is entered into the LIU during system initialization via a command message.

The elapsed time (Δt) may be exceeded for two reasons. One possibility is excessive time delays on the FI due to bottlenecks. Since prevention of bottlenecks is one of the key features of the FI system, this possibility is unlikely. The other possibility, assuming the pre-established value has been selected properly, is that an intruder has recorded some messages previously distributed by the FI and is rebroadcasting those messages. The LIU detects these rebroadcasted messages because of the excessive time difference between the generation of the original message and the reception of the rebroadcasted message.

Upon completion of the System Time check, control of the received message is given to the PSI output procedure.

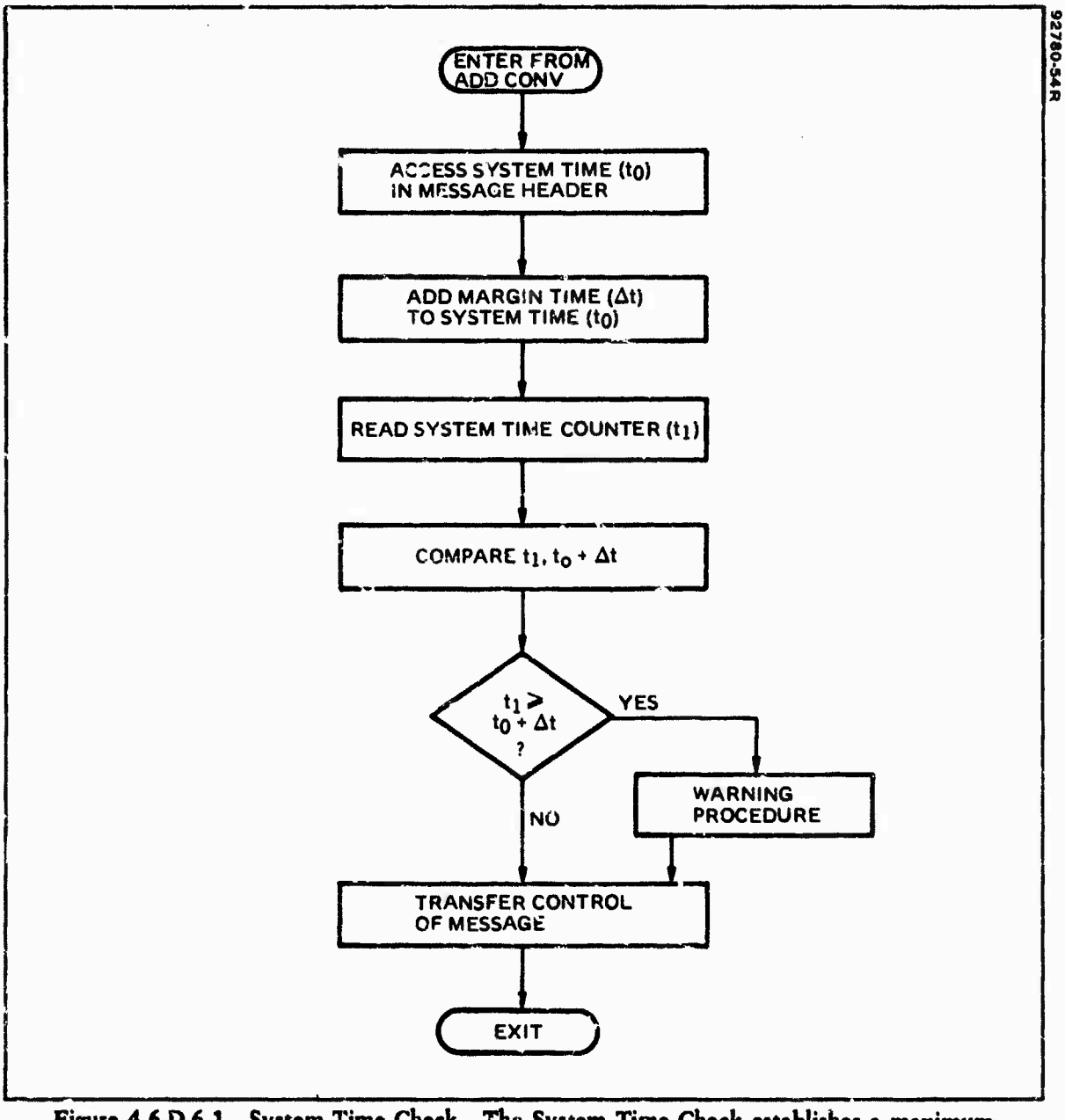


Figure 4.6.D.6-1. System Time Check. The System Time Check establishes a maximum desired elapsed time between message generation by a source DTE and message reception by a destination DTE.

1. OVERVIEW OF LIU FUNCTIONS FOR LIU OUTPUT TO DTE

The methodology of data transfer from LIU to DTE is the dual of the methodology of data transfer from DTE to LIU, with the exception of a programmed "wait" which allows the DTE to perform an error check on the received message.

The PSI output process is given control of a message after the message passes all checks and after all modifications are completed. The LIU transfers a message to its associated DTE via the PSI and then waits a predetermined, but variable time interval for a request for retransmission message from the DTE.

In transfers to the DTE, the DTE and LIU participate interactively in a standardized asynchronous transfer methodology. This is the dual of the methodology for transferring messages from the DTE to the LIU.

The LIU uses the control lines of the PSI to initiate message transfer and to indicate the beginning and end of message. The data word count (C) in the fourth word of the message header provides the LIU with the required message length information. The DTE uses the control lines of the PSI to control the instantaneous transfer rate.

If, after receiving a message from its associated LIU, the DTE finds the message unacceptable due to errors, the DTE generates a command error message which requests the LIU to retransmit the message. After each message transfer, the LIU waits a time interval, T_{ec}, for an error message. If no error message arrives within T_{ec}, the LIU erases the previously transferred message and then transfers the next message across the PSI to the DTE. If an error message does arrive within T_{ec}, the LIU retransfers the old message to its associated DTE and generates a command error message addressed to the FI manager.

The time interval, T_{ec}, is programmable. It is based upon the processing speed of the LIU's associated DTE and is placed in the LIU at system initialization or during system reconfiguration via a command message.

Some DTEs may not be interested in message header information or may be unable to use the message header information. In these cases, a DTE can request that its associated LIU never transfers a header across the PSI. In responding to such requests, the LIU removes the header from every message and transfers only the data section. (See Figure 4.6.E.1-1.) These cases are referred to as the "prefix header" case.

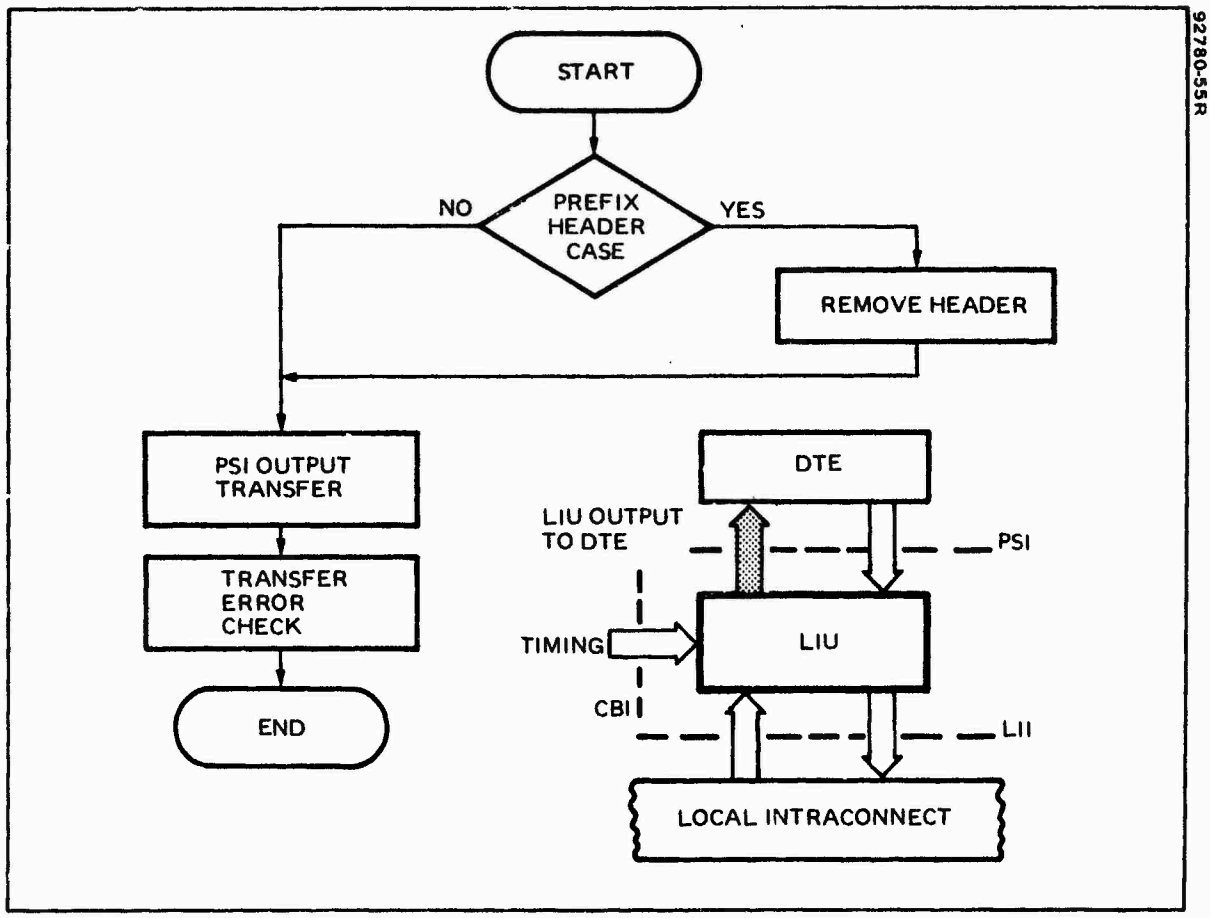


Figure 4.6.E.1-1. LIU Output to DTE. The transfer error check assures the validity of a message transfer to the DTE.

1. LIU FUNCTIONAL BLOCK DIAGRAM

The use of dedicated logic for message gating and microprocessor technology for message processing supports the high interface data transfer rate requirements while maximizing LIU flexibility.

The LIU transfers messages between the DTE and the LI. During these transfers, the LIU performs checks and modifications to the messages. To enhance LIU flexibility in executing these functions, the use of special or dedicated circuitry is avoided wherever possible. However, high speed, dedicated logic is required on the LIU side of both the PSI and the LII (see figure). Messages are transferred across the PSI at 180 Mb/s and across the LII at 90 Mb/s. While these rates require the use of dedicated logic, the parallel (18-bits wide) nature of these interfaces allows the use of existing and well established technology. Microprocessor technology is used for all other tasks performed by the LIU, including control of the message transfers. At the PSI the microprocessor sets up the conditions of message transfer; at the LII, the dedicated logic responds to timing information supplied by the LICU via the CBI.

The LIU contains a RAM to store messages being transferred between the PSI and the LII. When receiving messages from its associated DTE and when receiving messages from other LIUs, the LIU performs several checks and modifications. Since these checks and modifications need not be performed at the transfer rate of the PSI or of the LII, this message processing is performed by a microprocessor affording the LIU maximum flexibility.

The routines for the microprocessor, stored in read only memory (ROM), both the sequence of message processing events and the error procedures. As a result of the microprocessor implementation, changes in operational procedure do not necessitate a redesign of the LIU. The LIU has the flexibility to adapt to an addition or deletion of a message modification, the redefinition of an error procedure, or even a restructuring of the message header.

The LIU contains additional RAM to store information required for the various message checks and modifications. Stored are address conversion tables, authorization lists, current message numbers, and assigned sequence numbers (the LIU only stores information pertinent to its associated DTE).

Besides the dedicated logic required for message transfer, the LIU has several additional groups of dedicated logic. These are the error check logic, the memory status logic, and the System Time counter. The error check logic performs a longitudinal parity check on all messages while the memory status logic computes the availability of space in the RAM message store and reports the results to the LICU. The System Time counter maintains the correct value of System Time.

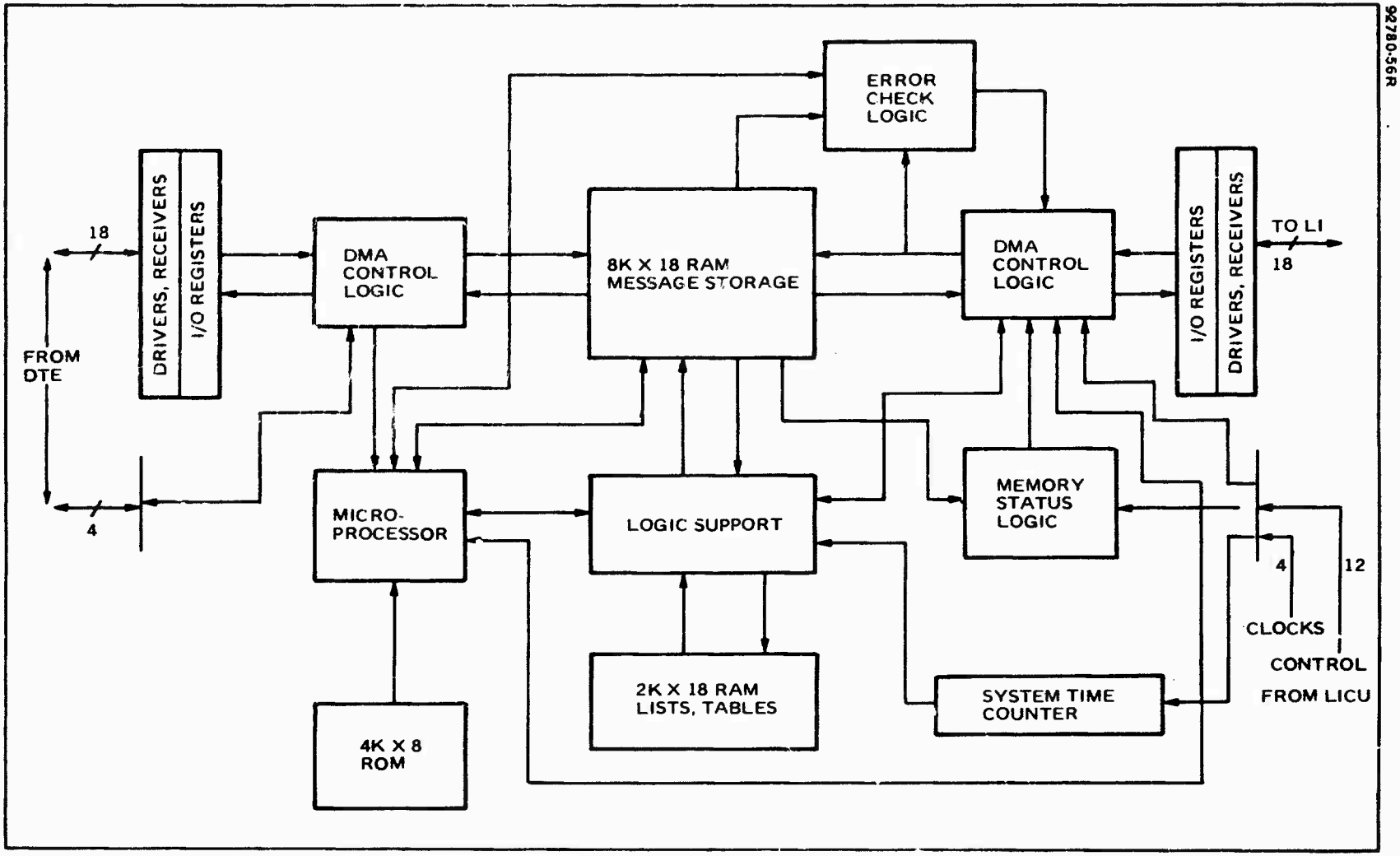


Figure 4.6.F.1-1. LIU Hardware Block Diagram. The LIU performs transfer functions between the PSI and the LII with a minimum of special circuits.

SECTION 7
EXTERNAL INTRACONNECT UNIT (EIU) DESCRIPTION

Part 4 – Task III, Preliminary Design Analysis
Section 7 – External Intraconnect Unit (EIU) Description

1. EIU FUNCTIONAL BLOCK DIAGRAM

Four functional areas of the EIU provide a gateway for asynchronous message transfer between the LI and EI, and generate timing signals for the EI. Implementation of the EIU with state-of-the-art technology provides for negligible development risk.

As shown in Figure 4.7.1-1, the functions performed by EIU can be partitioned into four areas: the message buffer and transfer control, the Key Generator (KG) interface controls, the fiber-optical transmitter/receiver, and the timing generator.

The message buffer and transfer control interfaces directly with the LI, providing message buffering, generating handshake controls, and controlling the EI timing configuration. Since the KG unit to be used for FI secure data transmission is not yet specified, the KG interface control will not be elaborated upon in this report. The fiber-optical transmitter/receiver performs optical to electrical signal conversion for reception and vice versa for message transmission. It also provides EI regeneration functions. The timing generator supplies transmit and receive timing and clocks.

The interface with the LI involves 18-bit data reception and transmission in a half-duplex mode. Message reception is under the control of the control bus (12 lines). The EIU categorizes the sequence of received VB or LS messages and retransmits them on the appropriate bus slots. The EIU also receives external memory status reports from each local LIU for the front-end handshake of the external message transfer.

Separate transmission and reception buffers are used in the EIU. The capability of simultaneous data store and read out at different memory locations is a highly desirable feature for optimizing memory size and reducing transmission delay, since the message can be read out for re-transmission shortly after having been received.

The local and external transfer handshakes are two different processes. The local handshake involves generation of reservation requests, transmission enable sensing, outbound message detection, and ACK/NACK reception. LI handshake is carried out over the control bus and on the 18-bit data bus. External handshake includes message counts, transfer request, transfer grant, and ACK/NACK. Since EI handshake is carried out via the EI, the EIU incorporates the transfer handshake into the timing structure.

The fiber-optical transmitter and receiver performs electrical to optical and optical to electrical signal conversions at the 20 Mb/s data rate. For a 60 Mb/s EI capacity, three fiber-optic channels each are provided for transmission and reception. In addition to data transmission and reception, the unit also regenerates all signals on the EI, thus providing a repeating function at each shelter.

The timing generator synchronizes to or generates External Intraconnect timing for the transmit and receive buses. Each EIU has the capability to automatically generate EI indicator timing or sync to another EIU. The functions

include generation of cycle time, slot time, clock pulses, time acquisition sequence correlations, detections, and timing compensation. The timing generator is capable of coordinating with message buffer and transfer control functions to perform external timing configurations.

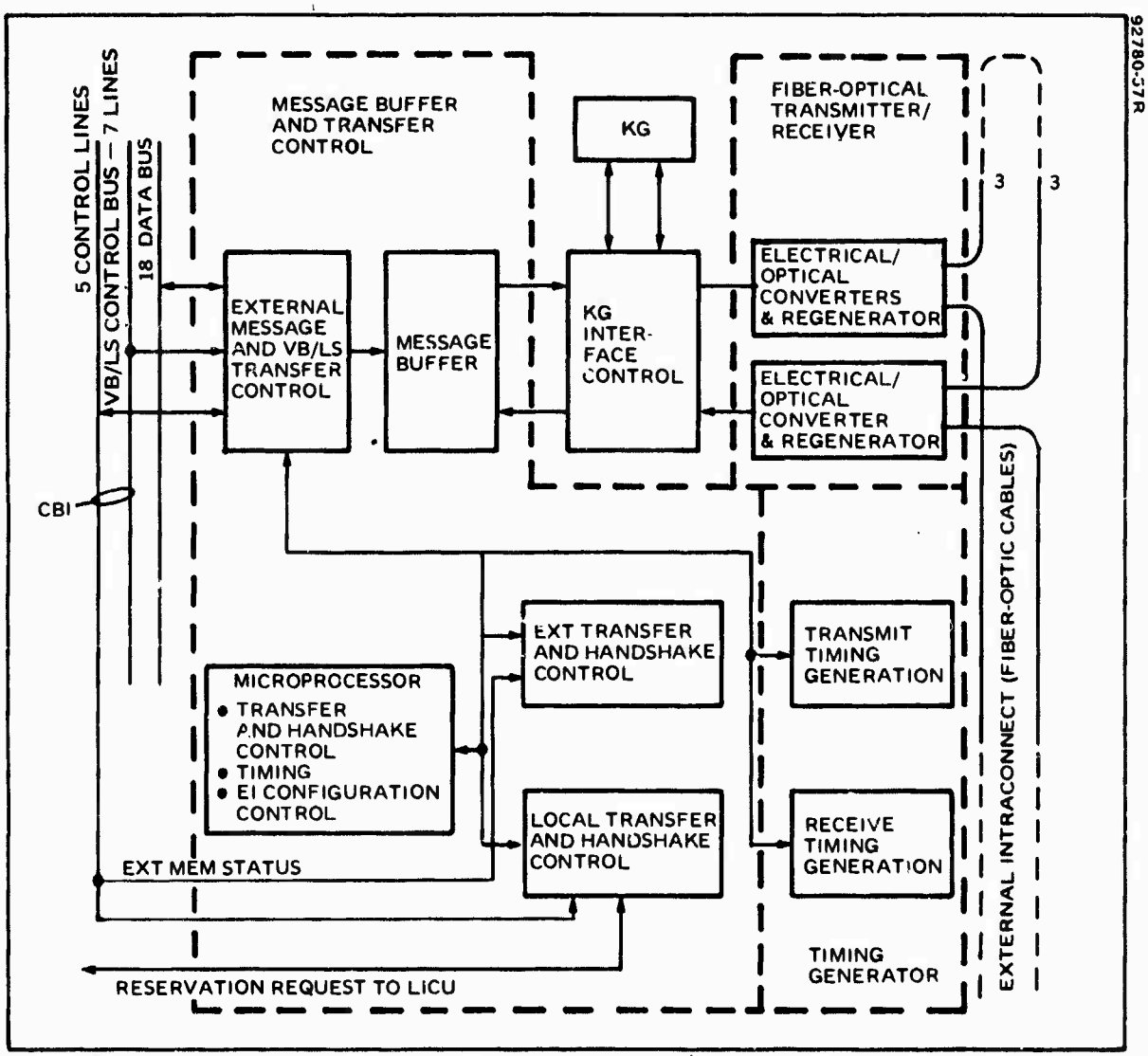


Figure 4.7.1-1. The EIU Functional Block Diagram. The functions are performed by discrete ICs or by a microprocessor, depending on the processing speed required.

2. IMPLEMENTATION OF EIU MESSAGE BUFFER AND TRANSFER CONTROL

Maximum use of microprocessors is made for medium speed and non-time-critical functions. Hi-speed gating and processing functions are implemented with discrete integrated circuits (IC).

The EIU message buffer and transfer control function is implemented with a microprocessor and discrete integrated circuit components as shown in Figure 4.7.2-1.

Line drivers and receivers serve the interface between the LI and EIU. The LI is an 18-bit wide bi-directional data bus requiring tri-state operation. The drivers must be capable of driving all the local receivers (LIUs, LICU and EIU) at a 5 Mb/s data rate.

Both input and output memories are shared by various types of messages providing greater flexibility and better memory utilization. For example lower V Band LS traffic provides more capacity for block message storage. Random access memory ICs (RAM) are used due to their large storage capacity, small physical size, high access speed, low power consumption, design simplicity, and availability. To provide memory sharing capability, a memory table indicating the beginning address and the length or the end address of a message storage is constructed for each message storage configuration. When a message is read out, the memory table is first read out as a pointer leading to the desired memory address. Simultaneous read-out and write-in can be achieved by use of an address register. After each word is written in the memory, the address is stored in the register. The read-out address is then loaded into the address counter to read out a word at the desired address. The RAM is actually operated as a FIFO. This capability enables message transmission during reception or vice versa.

A microprocessor is employed for lower speed or non-time critical processing. These include front-end handshake, timing acquisition computation, timing configuration processing, message count, reservation slot count, and transfer grant table generation. The configuration message received from the FI Manager requires pre-processing to convert it into a suitable form. These steps are carried out by the microprocessor. During timing acquisition, the necessary epoch detection checking, delay measurements, and timing compensation controls are also performed by the microprocessor. The LI external memory status table and the timing configuration data are generated and controlled by the microprocessor.

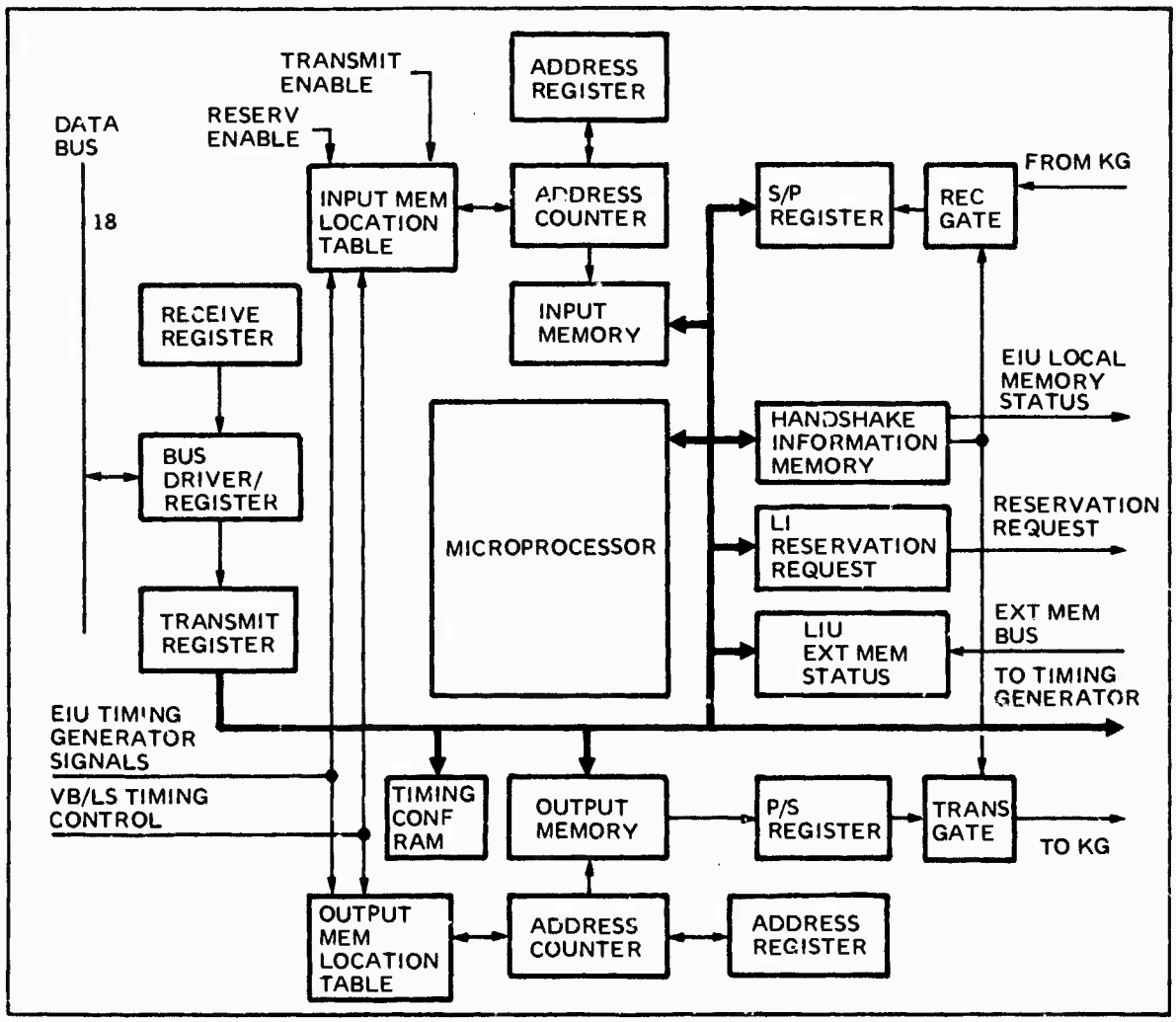


Figure 4.7.2-1. EIU Message Buffer and Transfer Control Block Diagram. Implementation exploits integrated circuits and a microprocessor to satisfy speed and flexibility requirements and to minimize hardware.

3. OPTICAL TRANSMITTER/RECEIVER

Data transfer using optical techniques provides high information-carrying capacity and low error rates over long distances.

Fiber-optical links are used as the transmission media for the External Intraconnect (EI). Transmission of messages on the EI is 3 bits in parallel on the transmit bus and 3 bits in parallel on the receive bus; each transmitted at 20 Mb/s rate on a single fiber, providing a total of 60 Mb/s capacity for the FI external intraconnect. Three sets of transmitters (for the transmit bus) and three sets of receivers (for the receive bus) are needed in each EIU for electro-optical conversion and regeneration (repeating) functions.

Passive coupling on the fiber-optic EI was not implemented because tapping of the EI by many shelters causes significant losses in optical power. Typical insertion losses are in the range of 2 dB from light source to fiber cable or from fiber cable to detector, and 3 dB for cable to cable splicings. (The insertion loss is a function of cable end preparation, numerical aperture, device geometrics, and termination technique.) In a re-deployment environment, higher loss could result from untailored connections and the difficulty of keeping the cable ends or connectors clean. In addition to insertion loss, there are cable and optical branching losses. Losses are a function of system configuration, dispersion and topology, and vary for different deployments.

The repeater function is built into the optical transmitters and the receivers. The signal is regenerated in each, yielding point-to-point optical links. In order to prevent possible disruption due to power failure, disability of the transmitter or receiver mechanism or shelter loss, a bypass fiber-optical link is provided. This link assures the continuation of the optical waveguide even though the repeater function is disabled. The bypass is long enough to reduce its vulnerability to shelter-directed enemy action. The delay of the bypass is made the same as that of the repeater to assure the signals at the point-of-joint are coherent in the "bit" sense (not in the light coherency sense). Figure 4.7.3-1 depicts the configurations of the transmitter and receiver.

The optical signal transmitted from the previous EIU is received, converted into an electrical signal and then converted back to an optical signal for re-transmission. During the transmission time of the EIU, the multiplexer between the two converters switches to the transmit message buffer for local message transmission. Since in the TDMA format only one subscriber transmits at a time, there is no other signal on the optical waveguide. The transmitter converts electrical signals into optical signals for transmission on the optical waveguide. The electrical signal which drives the optical source is TTL compatible. The signal waveform is baseband digital.

The receiver structure (for the receive bus) is identical to that of the transmitter except that a signal path to the receive buffer is provided for incoming messages.

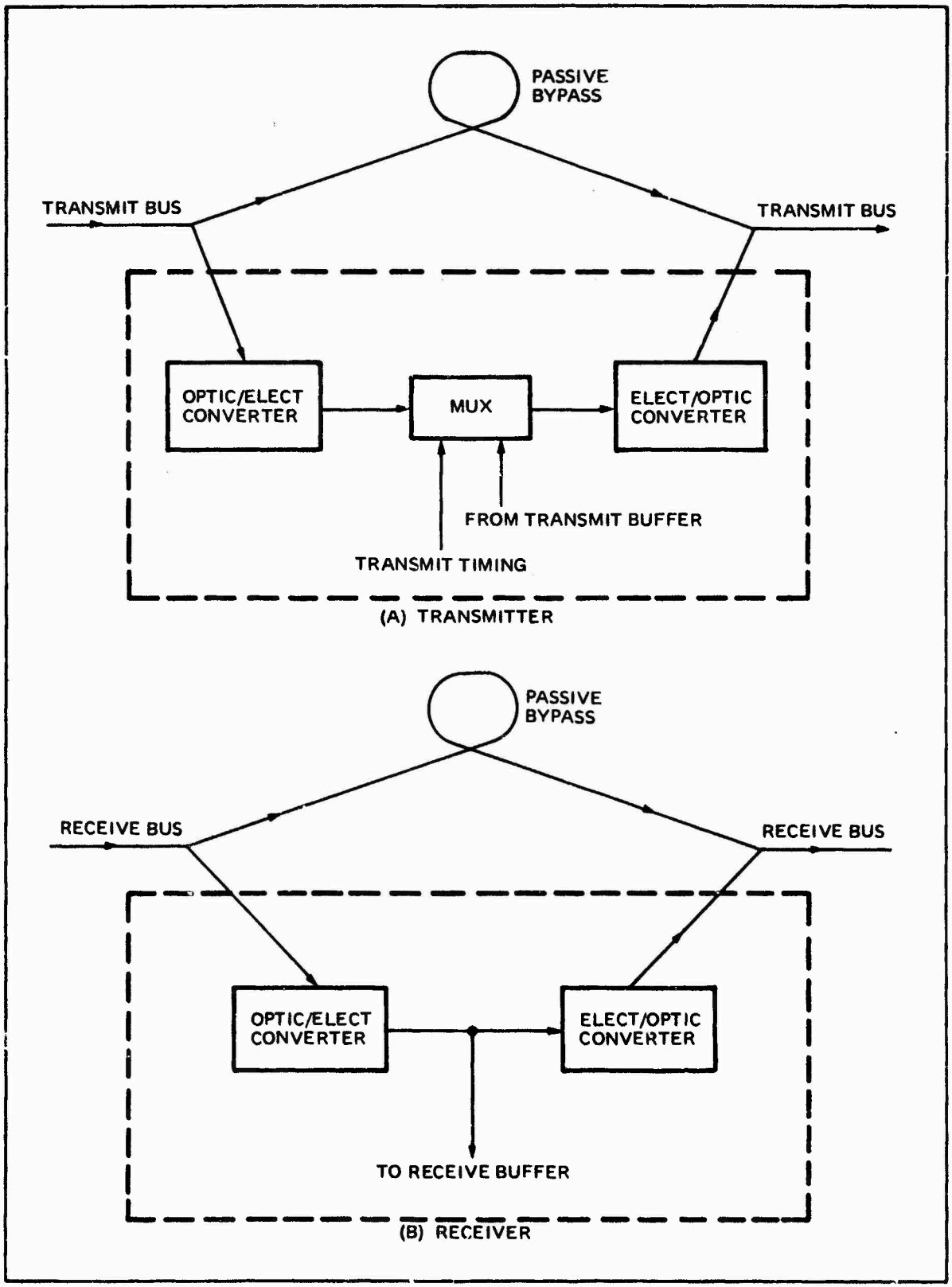


Figure 4.7.3-1. Optical Transmitter and Receiver Block Diagrams

4. GENERATION OF EXTERNAL TIMING

Flexibility in EI configurations is provided through the use of programmable timing controls. External timing acquisition, as well as transmit bus and receive bus timing harmonization, are provided by the timing generator.

In order to maintain independence of the external and local timing, it is necessary to have an external intraconnect timing generator in each EIU. The timing generator under control of a microprocessor supplies all needed timing marks, clocks, and message transfer timing controls for the EI. The transmit and receive timing are supplied by two identical sets of hardware since compensation of propagation delay makes it necessary to use separate timing references for transmission and reception. As shown in the figure, the basic structure of the timing generator includes a clock source, a timing chain, and timing decoders. The timing chain receives pulses from the clock source and divides them down to the required period. Outputs of the timing chain are used for clock pulse generation and decoding. The timing chain clock is 10 MHz providing a timing resolution of 100 nsec. The timing chain is preset by loading bias for propagation delay compensation and epoch counts. Timing information is extracted from the timing chain by the microprocessor for computing spacings of consecutive epoch sequences and detecting the order of epoch numbers along with the order of polled addresses.

An epoch number register and sequence correlators are used for timing acquisition. The epoch sequence, generated by the master timer is stored in the register. (Any EIU may be designated the "master.") The EIUs determine the epoch by correlating the sequence from the master with their pre-stored epoch number.

Following the epoch correlation process, final synchronization is accomplished by use of an early-late gate correlation from which a timing bias is derived.

The timing decoding consists of basic decoding and programmable decoding. The basic decoding provides timing signals for essential system operations. It is fixed designed and is not affected by timing reconfiguration. Programmable decoding generates timing signals on the basis of operational needs such as VB and LS capacities, numbers of EIUs, and the length of the cycle time. The programmable decode function is capable of receiving configuration data and generates timing signals accordingly.

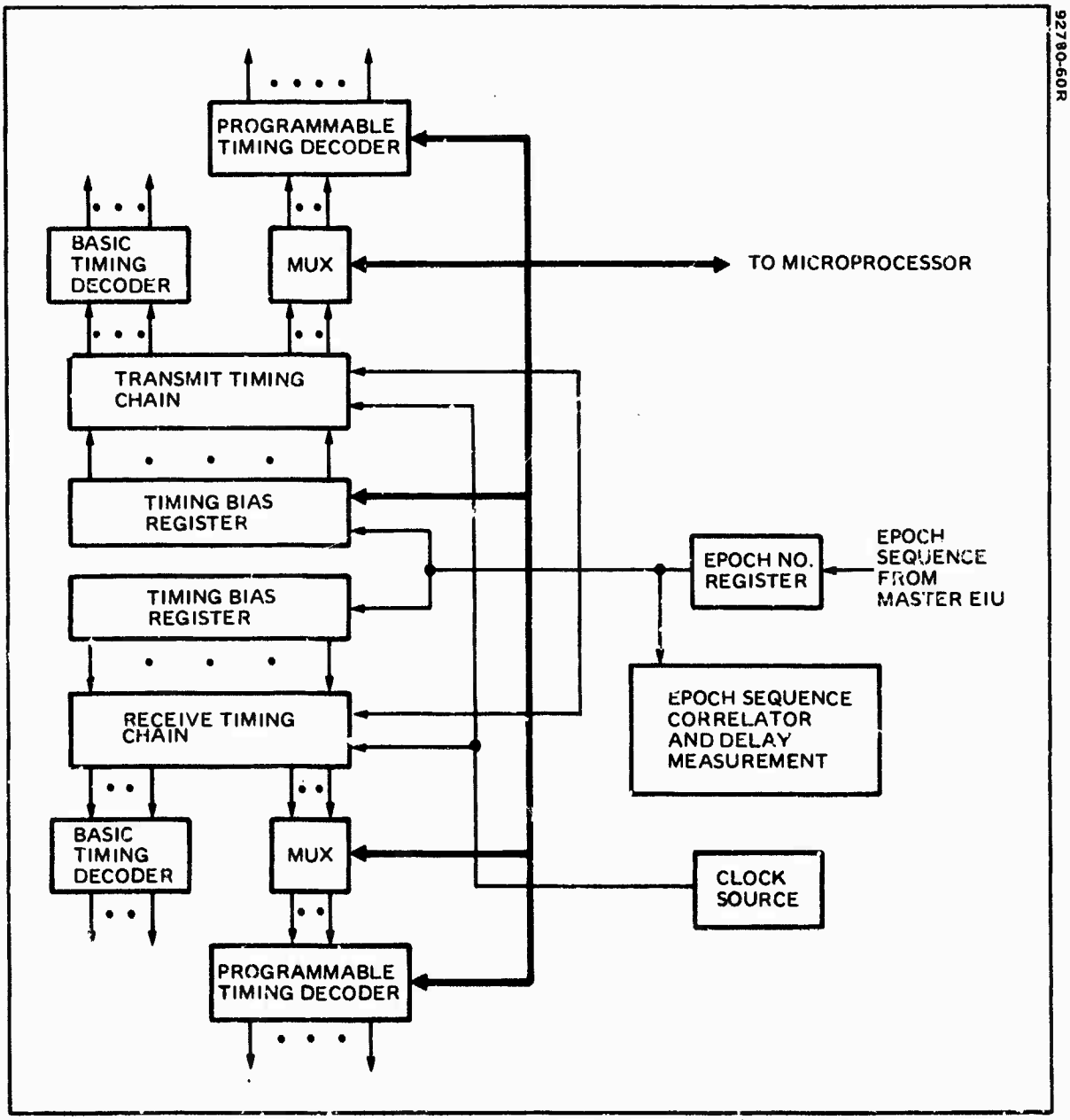


Figure 4.7.4-1. Timing Generator Diagram. Separate transmit and receive timing generators are required in order to compensate for propagation delay.

5. BLOCK MESSAGE TRANSFER: LI TO EIU

A dedicated message flow control line from the LICU simplifies receive procedures and optimizes the use of the EIU buffer.

The EIU receives Block messages from the LI in a sequence of steps controlled by the LICU as shown in the figure. Block messages can be broadcast or transmitted point-to-point and message length can vary up to 1040 (16 header plus 1024 data) 18-bit words. Reception is initialized by sensing the "outbound message" signal from the LICU. The use of a dedicated line for this purpose eliminates the need to constantly detect the destination address of each message transfer. The transmit enable line is always activated during the entire period while the message is being received. The sensing of the outbound message indicator sets a flag which in turn enables reception gating. The flag is reset when the transmit enable line is deactivated at the end of message transmission. Transfer gating is disabled during the local VB and LS bus times therefore temporarily halting Block message transfers. Block message transfers resume when the VB or LS slots are over. At the end of message transfer (unlike the LIUs) the EIU does not generate ACK/NACK since they are generated by the destination LIU.

Each word of the message received from the LI is loaded into a register before storing in memory. This allows time for the EIU to determine if the message is a timing configuration message or a Short Block message. In the case of the former, these messages are routed to a preassigned memory location which the microprocessor can access in when generating configuration data messages.

Short Block messages must be identified so that they can be stored in a manner which facilitates transmission in the Short Block message slots.

The memory is shared by all types of messages except the configuration message. When storing a message, the starting address and message length are loaded into a memory location table. Since the RAM memory is designed to be capable of simultaneous read and write (First In First Out fashion) it is possible to transmit prestored VB or LS messages while storing Block messages.

Message count, which is used in the front end handshake process, is incremented by one each time a message is received from the LI.

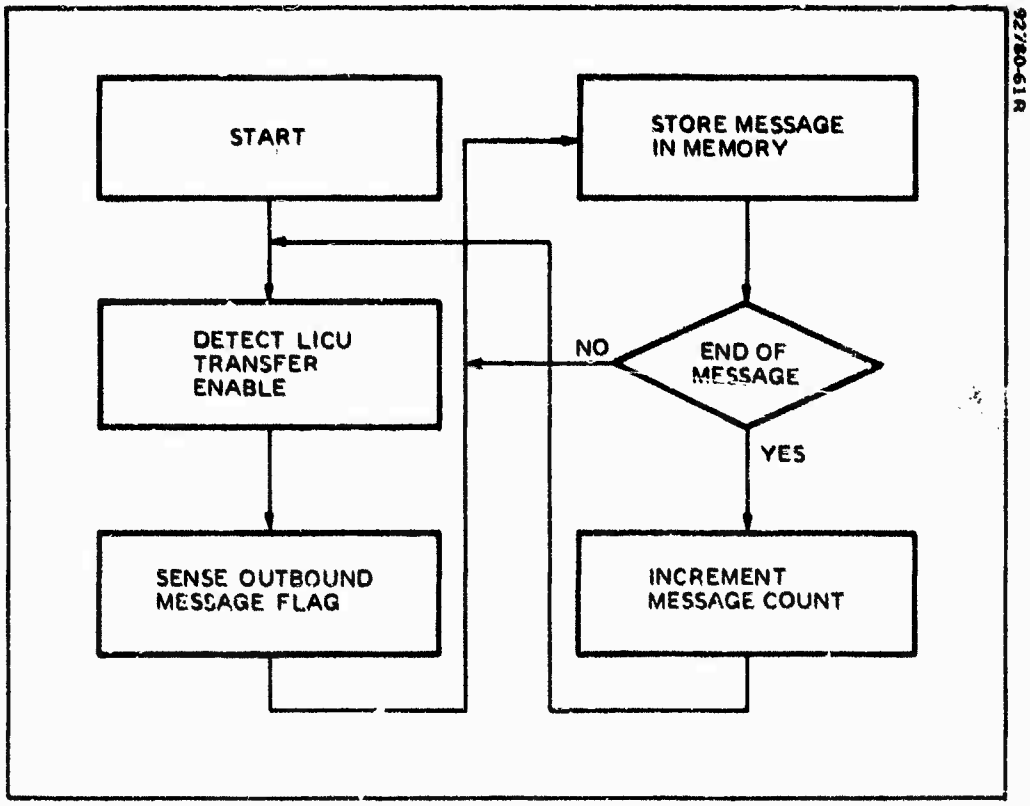


Figure 4.7.5-1. Block Message Reception From LI

6. BLOCK MESSAGE TRANSFER: EIU TO EI

Handshake controls which prevent bottlenecks and bus saturation problems are implemented within the microprocessor control structure of the EIU.

The EIU decides the number of Block messages to be transmitted in the forthcoming cycle. This task – the "handshake" – must be performed before the start of the cycle.

The first part of a handshake process is the message count (see Figure 4.7.6-1A). The message counts contain two parts: the EIU and FI message counts. The EIU message counts are generated in each EIU while the FI message count is the sum of the EIU counts generated by all the EIUs on the FI. The EIU message count is incremented by one whenever a Block message is received from the LI. The count is transmitted during the each EIU's assigned message count transfer slot and is received by all EIUs. Using these counts, each EIU generates a table based on the order of receptions. The message count table establishes the order of the transfer-request slots and message tran missions during the Block transfer time. An upper limit is set for the total message count for each cycle time. (A maximum number can be assigned to each EIU to assure that slots are more evenly distributed among the EIUs.) Once the upper limits are reached, no additional message counts are transmitted by any EIU.

The Short Block message transfer slots following the message count transfer slots provide adequate time for message count receptions and processing. During the 40 transfer-request slots (which constitute the first 40 message counts) the EIUs transmit transfer-requests, one for each message, to indicate destination address and message length. This information is stored by all EIUs. The transfer grant is sent by the destination EIU by indicating its address and approval of the intended transfer. (For broadcast messages, no destination address is transmitted and it is so indicated in the transfer-request.) Using the microprocessor, the EIU constructs a table containing message count, transfer-request, and transfer-grant. From the table, the microprocessor determines the availability status of all EIU receiver buffers, and the duration of each message transmission. During Block transfers, the transfer-request (which is granted by the destination EIU) enables the message transmission (Figure 4.7.6-2). Transfer-requests which are denied are skipped and the next request is examined for message transfer gating. This transfer gating process is based on the accumulated message count table, transfer-request table, and transfer-grant table.

The last step of message transfer from an EIU to the EI is the reception of ACK/NACK. The transfer-grant table is used again. The slot which corresponds to the order of the message transfer is gated for ACK/NACK reception. The received ACK/NACK is then passed back to the source LIU via the LI.

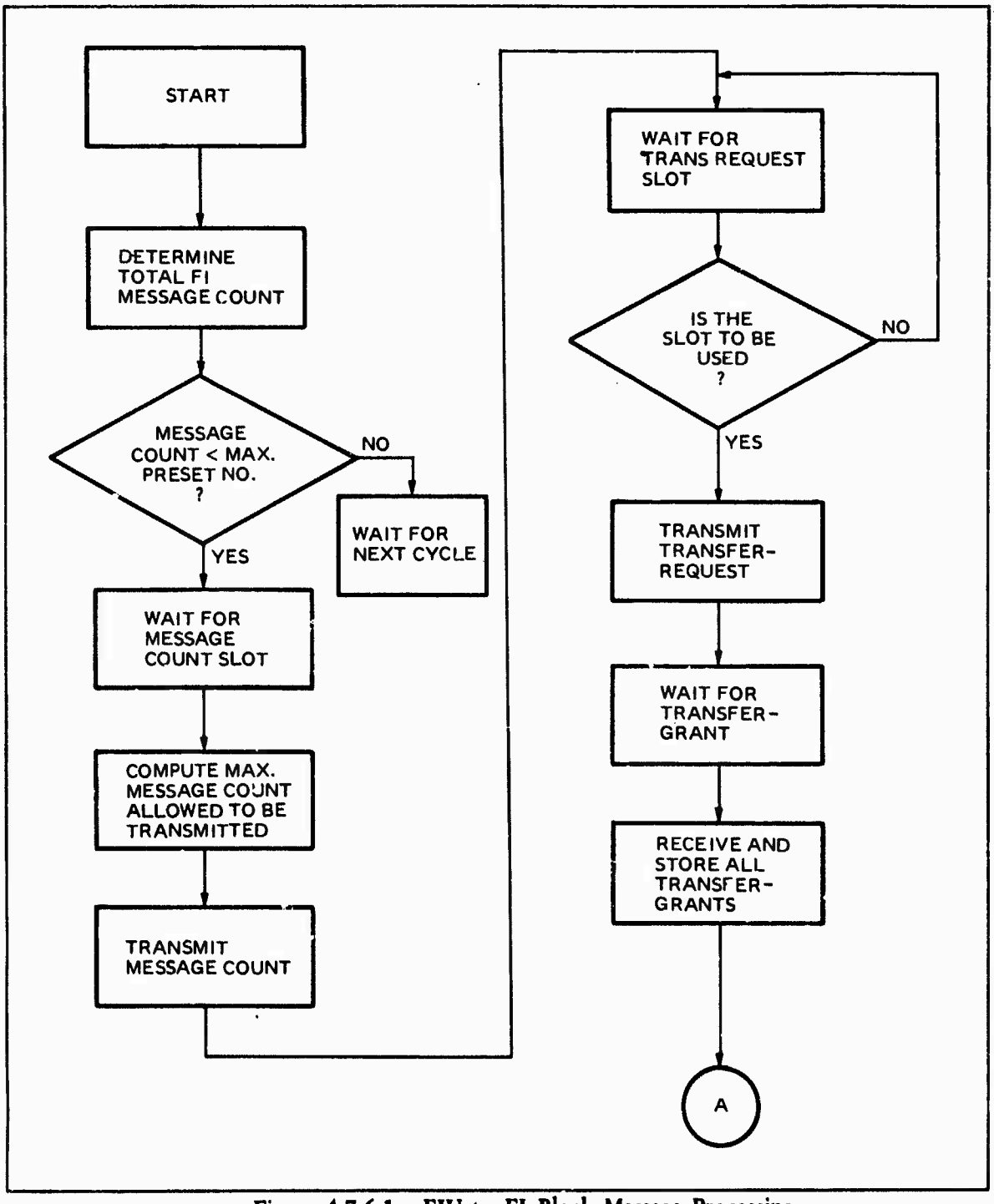


Figure 4.7.6-1. EIU to EI Block Message Processing

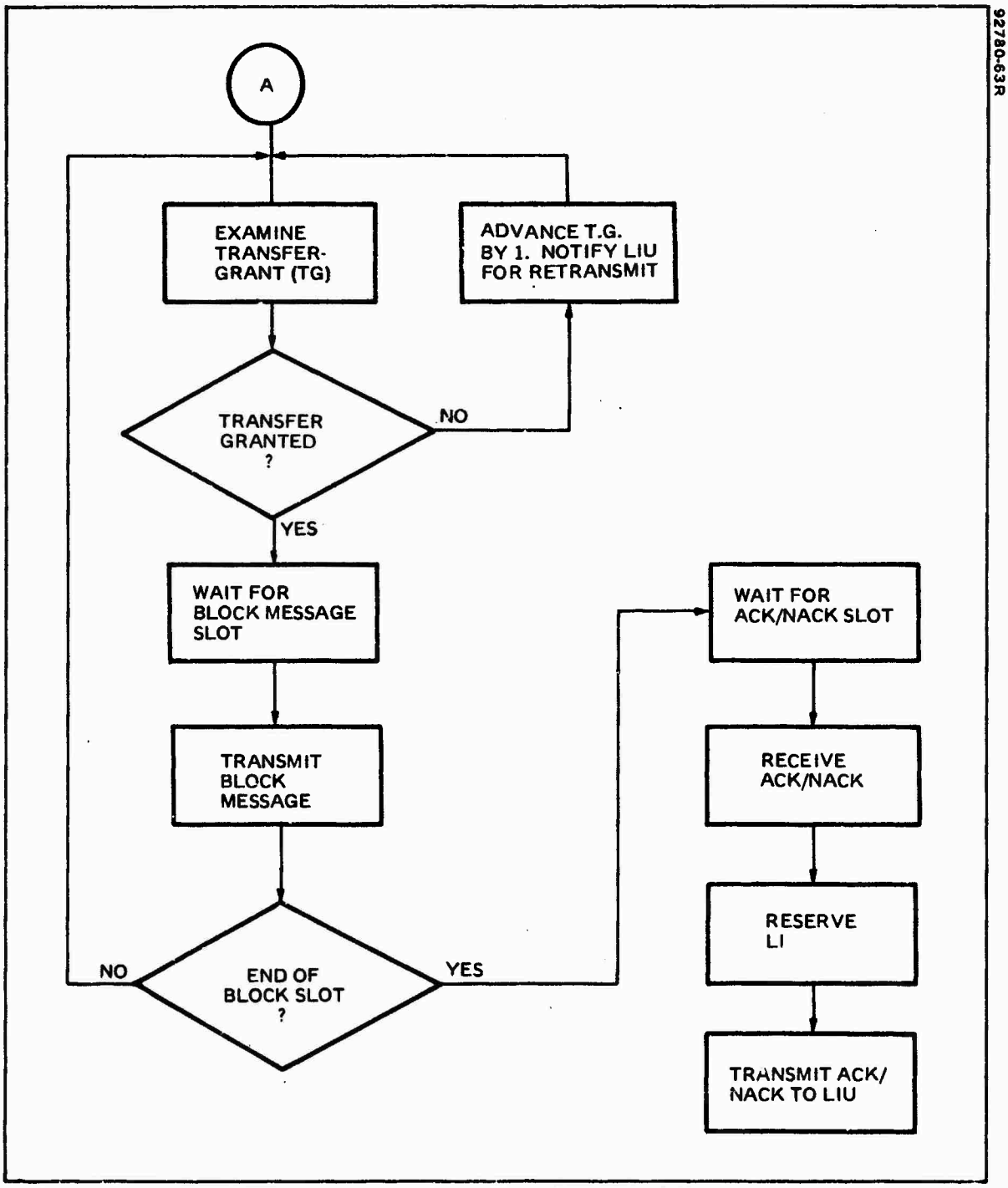


Figure 4.7.6-2. Block Message Transmit to EI. The external message transfer handshake imposes negligible overhead on external intraconnect capacity.

7. BLOCK MESSAGE TRANSFER: EI TO EIU

Reservations and handshake are accomplished in one EI cycle by the EIUs, utilizing this pretransmission information to reduce message transfer processing.

The EIU receives Block messages based on the timing structure and handshake controls. The Block message is transferred using distributed reservation control and transmitted during a time which is systematically constructed into the timing structure.

As shown in the figure, each reception is accompanied by handshake procedures. During each cycle, the transfer-request (which indicates the destination address and the message length) are stored by each EIU. A table is generated to indicate the length of each message, and whether the message is to be transmitted or received. (For broadcast messages, only the message length is stored.) The reply to transfer-request is delivered via the transfer-grant slots. Transfer-grants from all EIUs are stored and a table is generated which matches the transfer-request table. During the Block message transfer time, the EIU reads out the first transfer-request and transfer-grant from the tables for the first message reception. If the destination address matches the EIU address and the transfer is granted, or the incoming message is a broadcast message, reception is enabled. If the destination does not match the EIU address, the incoming message will not be stored. If the destination address matches the EIU address and the transfer is not granted, the message will not be received and the EIU will read the next reservation.

All EIUs use identical steps for Block message reception. The reception control, the transfer-request and transfer-grant tables are generated by the microprocessor in advance. As a result, real time detection of destination addresses from the message header is avoided and high speed special hardware for address detection is not needed. The reception control table is implemented with a simple random access memory (RAM) with incremental addressing.

The received Block message is entered into a memory organized to provide FIFO type operation. The addressing scheme is identical to the memory structure for message transfer from LI to EI as described in previous topics.

The last step of the Block message transfer is the ACK/NACK transmission. The ACK/NACK is generated by the destination LIU at the end of each message reception. The ACK/NACK is received by the EIU associated with the destination LIU (i.e. the same shelter as that LIU) and is transmitted to the source LIU during the ACK/NACK slots of each cycle. Routing of the ACK/NACK transmission is accomplished by use of the transfer-request and transfer-grant tables. The ACK/NACK provides a positive status feedback of the received discrete addressed Block message and also offers an efficient way of requesting message retransmission.

At least one Short Block message slot is assigned to each EIU for quick response messages, such as control messages. They are included within four groups in the EI timing structure, providing a time buffer between interactive handshake transmissions. They are processed within each EIU as Block messages, except that they are transmitted on the External Intraconnect in assigned slots.

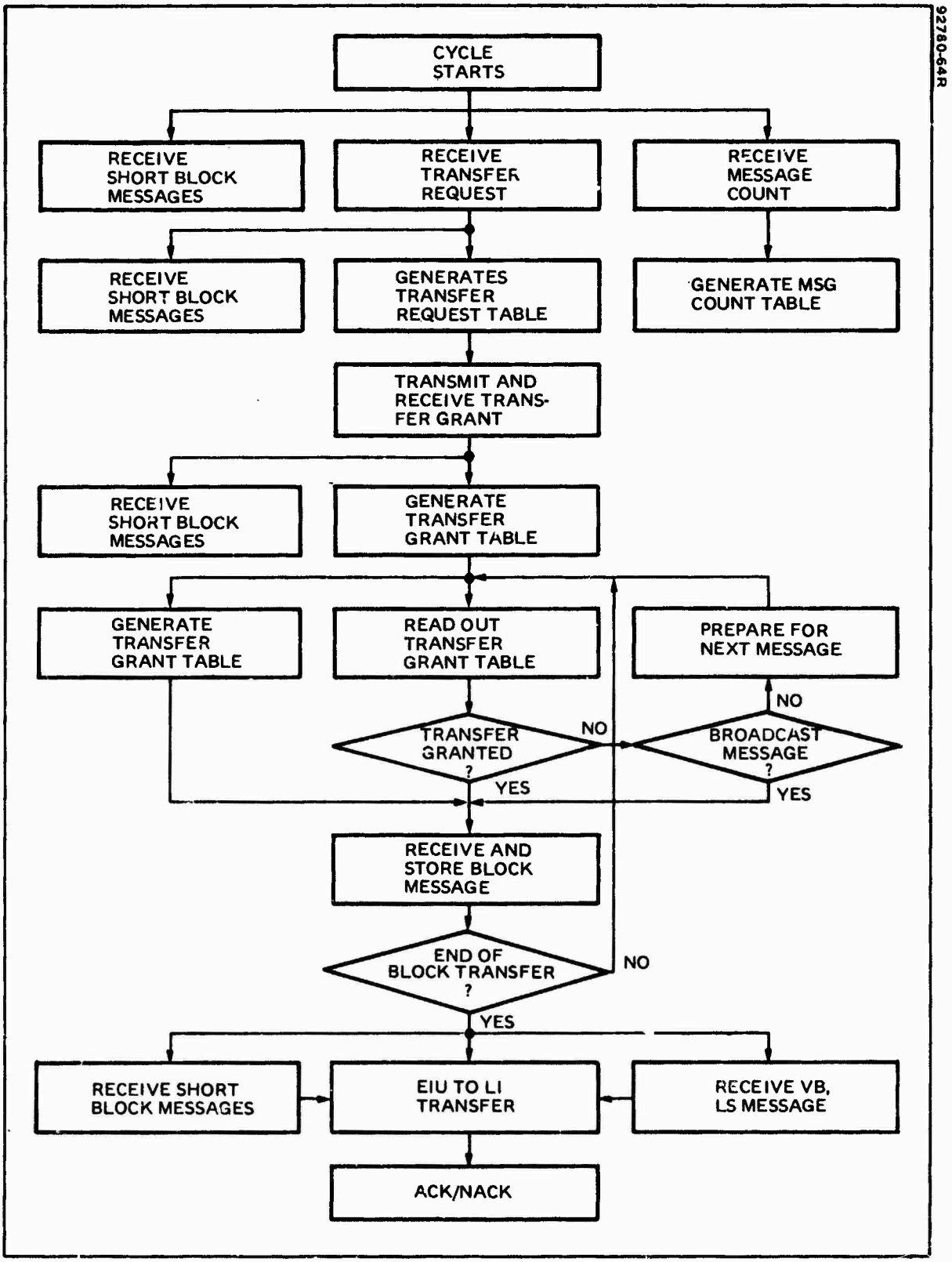


Figure 4.7.7-1. Block Message Receiption From EI

8. BLOCK MESSAGE TRANSFER: EIU TO LI

The EIU is given priority over LIUs in accessing the LI. This assures that external messages will be removed from the EI rapidly.

Messages received by the EIU from the EI are stored in a buffer memory to ensure that there is no dependence of timing between the EI and LI. The buffer is designed to provide a smooth data flow between the two separate timing systems and two types of transfer protocols (LI to EIU, and EIU to EI).

At the beginning of a message transfer, the EIU microprocessor starts processing local LI reservations (see figure). The processing includes message length tabulation and reservation-request generation. Message length tabulation is a word count extraction from the message header, readily obtained from the message stored in the memory. The message length (word count) which is used by the EIU to determine the end of message transfer is stored in a counter.

To transfer messages to the LI, the EIU generates a reservation-request which is transferred to the LICU via a dedicated line. The request causes the LICU to grant message slots to the EIU at the earliest possible time. The delay, caused by the processing time of the microprocessor and the LICU set-up time, must be kept short in order to achieve a fast message transfer and ACK/NACK reply. The delay is crucial to the ACK/NACK function designed in the external timing structure since the ACK/NACK must be received from the LIU and retransmitted by the EIU within one external cycle time. (This fast turnaround requirement can be relaxed by providing a longer time between the block message transfer slots and the ACK/NACK slots when configuring the external timing.)

After the reservation-request, the EIU waits for a transfer enable from the LICU. When the transfer enable is activated, the first word (containing the EIU address) is placed on the 18-bit data bus by the LICU, enabling the EIU message transmission to the LI. During the message transfer, the reservation-request line from the EIU stays activated. At the end of the message transfer, the reservation-request is deactivated but the transfer enable from the LICU stays activated to provide adequate time for the destination LIU to perform error checking. The result of the error check is transmitted by using the last word before the transfer enable is deactivated as the ACK/NACK. Additional reservation-requests must be made by the EIU for more message transfers.

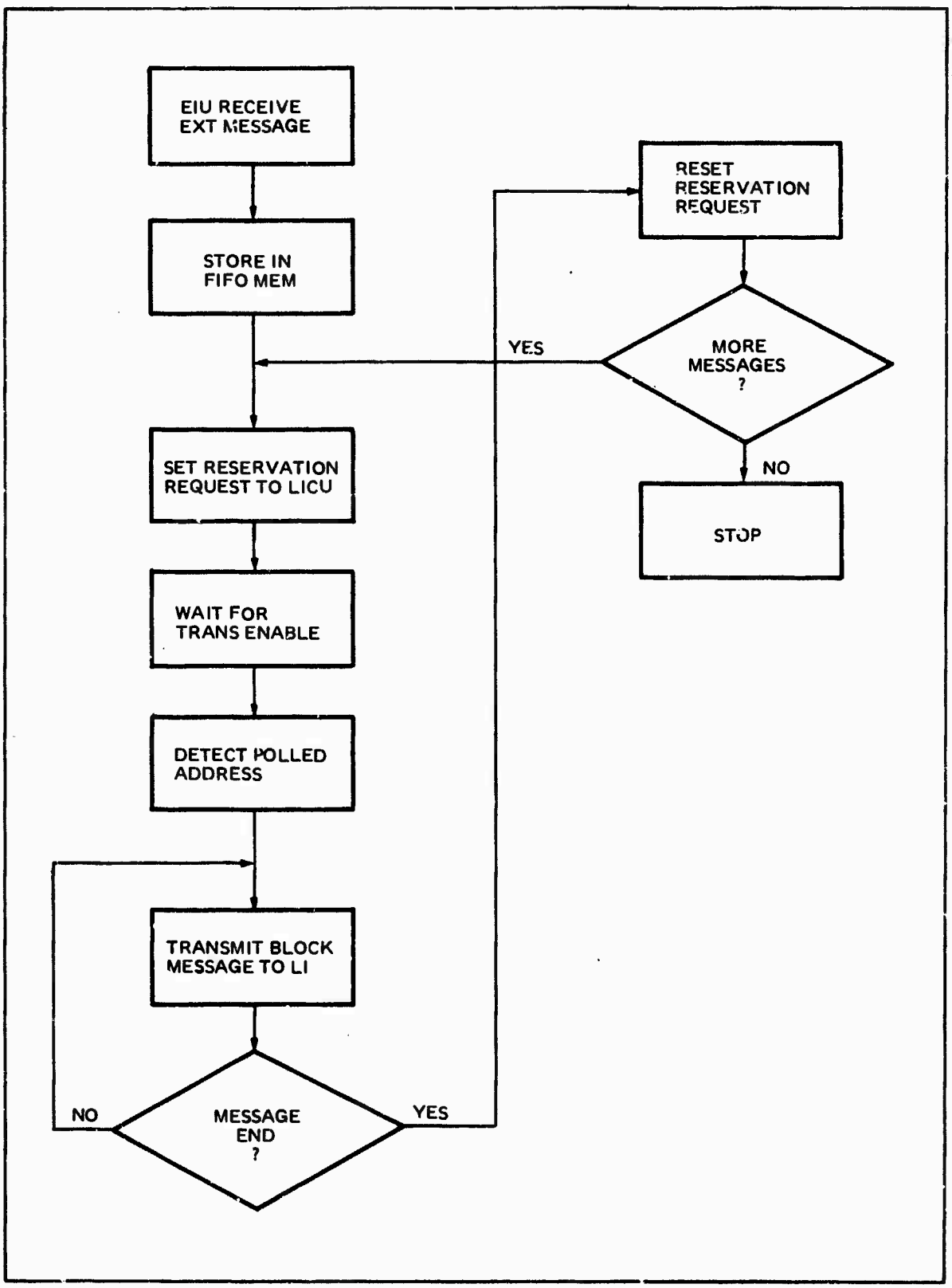


Figure 4.7.8-1. Message Transmission From EIU to LI. A dedicated line for reservation requests from the EIU to the LICU enables EIU to obtain high priority for local message transfer.

9. VIRTUAL BUS AND LAZY SUSAN MESSAGE TRANSFERS

The EIU control logic transfers VB and LS messages between the EI and LI in accordance with Sequence Numbers located in the message headers.

Assigned slots are used to transmit VB and LS messages. The slots of each of the VB or LS buses are assigned uniformly in the timing structure with a duration conformable to the message length. Transmission and reception are completely determined by the preset group of slots. While a basic time slot structure for Block, VB and LS messages is designed into all EIUs and LICUs, the FI management function can determine VB and LS time slot assignments to fit the application.

In both the Local and External Intraconnects, the VB and LS slots are assigned based on the bus capacity and message length. For example, for a 100 μs Local Intraconnect cycle time, a bus with a capacity of 10 Mb/s requires a slot repetition rate of one slot per cycle to transfer messages 1000 bits long. Therefore, the repetition rate and the message length uniquely determine a VB or a LS bus.

Control of a bus can be assigned to a DTE by the FI Manager or requested by the DTE and granted by the FI Manager. For that VB, the DTE may further assign portions of the bus capacity to other subscribers for message transmission by use of the Sequence Number scheme.

VB messages are received by all VB participants. A VB participant may both transmit and receive, or receive only. LS message transmissions are prescribed in a preset sequential order which is based on the Sequence Number assigned to each participant. LS participants may modify the message and retransmit it. Ultimately, the message returns to the originator after the completion of the time-ordered loop and is then taken off the bus by the originating DTE.

VB or LS messages are transferred via the LI and EI. On the LI side, as shown in the figure, the EIU detects VB and LS time slots generated by the LICU. The LS and VB control provides VB and LS bus numbers via the 7-bit VB/LS Control Bus. All VB and LS messages originating on the LI are received by the EIU which stores the messages in memory. The storage location and the bus number are used to generate a table from which the message can be recovered for the transmission to the EI. For EI transmission, the EIU detects the VB and LS slots from the EIU timing generator and reads the message from the memory for transmission during the appropriate VB or LS slots. The order of message transmission on each bus is maintained by the EIU by detecting sequence numbers from VB and LS message headers.

When an EIU receives VB or LS messages from the EI, the EIU detects the VB or LS slots from the EIU receive timing generator. All VB and LS messages are received and stored in the EIU receiving memory. A table which stores the memory addresses and the corresponding bus numbers is generated. The EIU detects the VB and LS bus numbers from the LICU control bus, locates the message in memory, reads them out and transmits in the appropriate local VB or LS slots on the LI.

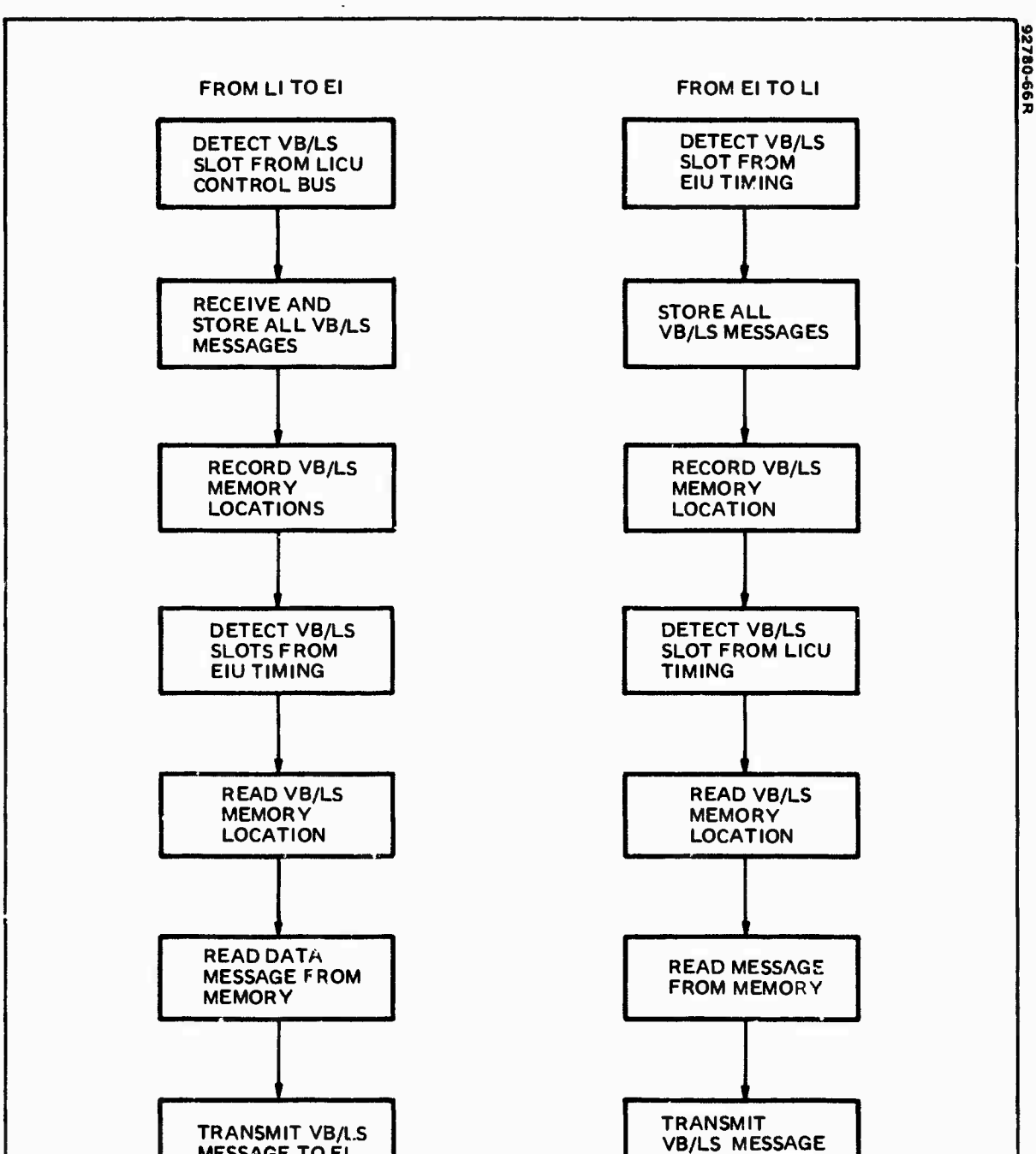


Figure 4.7.9-1. VB/LS Message Transfer. The EIU transfers VB and LS messages between the Local and External Intraconnects and maintains their sequential order by sensing Sequence Numbers in their headers.

SECTION 8
LOCAL INTRACONNECT CONTROL UNIT (LICU) DESCRIPTION

Part 4 – Task III, Preliminary Design Analysis
Section 8 – Local Intraconnect and Control Unit (LICU) Description

1. ALLOCATION OF FUNCTIONAL REQUIREMENTS TO THE LICU

A centralized unit for control of the EIU and LIUs within one shelter is possible because of the extremely short distances separating these elements.

In the FI design of Hughes, the LIUs, the EIU, and the LICU data and control interfaces are separated by inches. This results in such advantages as high transfer capacity and negligible bus propagation times, and the opportunity to perform control and timing functions in a common unit rather than in each LIU. The common unit is the LICU. Its functions and its interfaces are illustrated in Figure 4.8.1-1.

The LICU maintains control of the LI by controlling LI timing and all message transfers on the LI. It generates timing signals that control the operations of the LIUs and the EIU, allocates LI time slots to the three message transfer systems of the LI (Block Message, VB, and LS.), and coordinates and controls access to the LI by LIUs and the EIU. When Block Messages are to be transferred it implements a front-end handshake.

The LICU performs its control and timing functions according to configuration data stored in its memory. A basic configuration which determines its operation at start-up is permanently stored in each LICU. (The LICU also responds to reconfiguration messages from FI management by storing reconfiguration data and control and timing functions are then performed according to the new configuration.)

The LICU exchanges control and response messages (such as status and configuration messages) over the LI. Block message reservation requests and grants are also communicated in the LI timing structure (described in Section 4.4). Reservations are coordinated by Reservation Enable and Transmit Enable control signals sent to all LIUs and the EIU via the Block message control bus. Memory status reporting and control also takes place over the Block message control bus. The VB and LS bus designation and timing signals are transmitted via the VB/LS control bus to all LIUs and the EIU.

Basic system timing signals for the LI are also generated by the LICU. They include word, cycle, and epoch clock pulses and a 1-microsecond System Time (ST) clock used by LIU System Time counters.

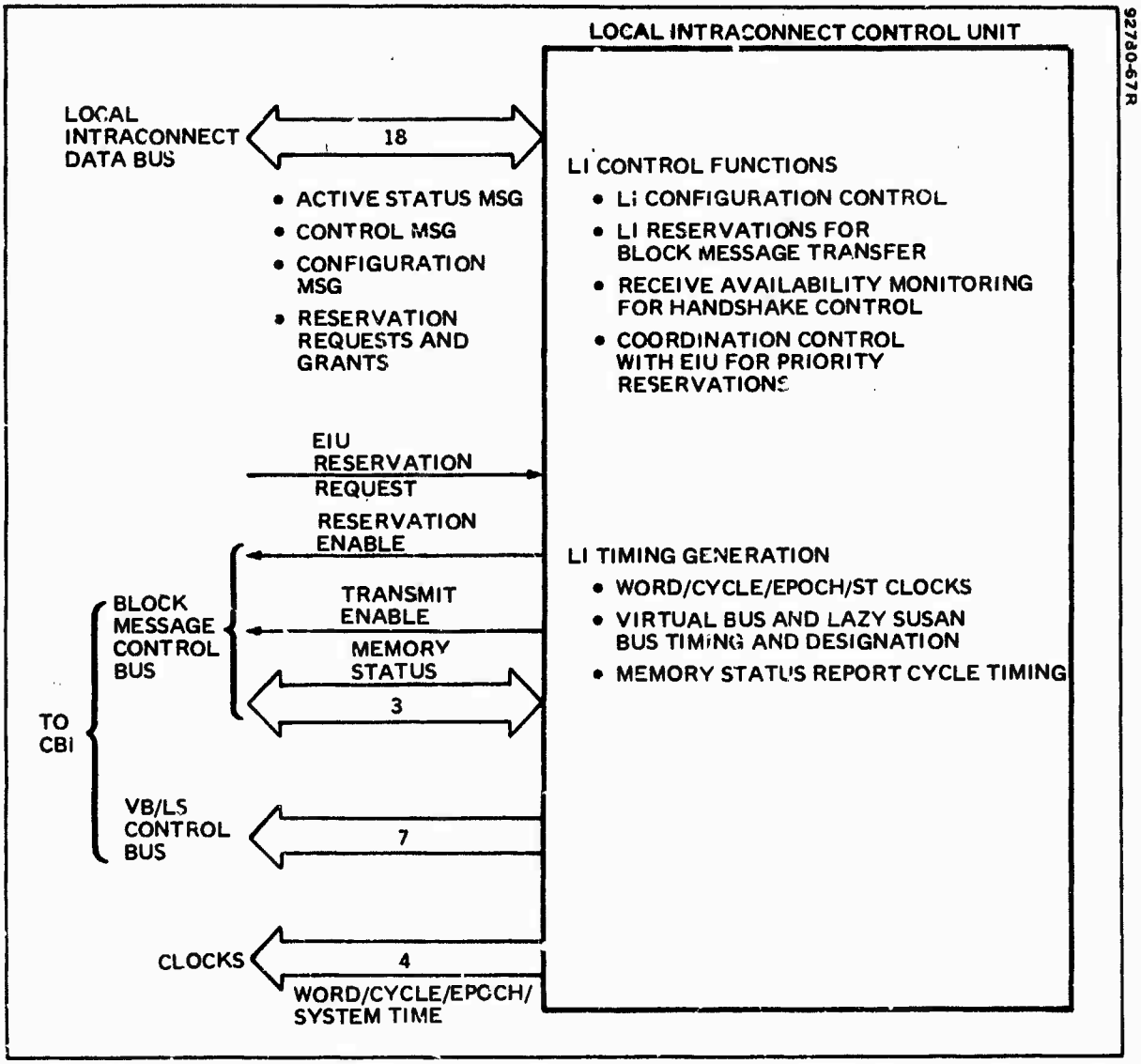


Figure 4.8.1-1. LICU Functions. Control and timing functions coordinate LIUs and EIU in message transfers and respond to RI management reconfiguration messages.

2. LICU IMPLEMENTATION

A microprocessor is used to support most LICU control functions; discrete circuits are used for high speed processing.

The control functions supplied by the LICU are LI interface control, front-end handshake, and reservation and message transfer control. These functions are realized either by a microprocessor or by discrete ICs depending on the processing speed required. (See Figure 4.8.2-1).

The reservation control process is established by the microprocessor based on transfer status and message count information. Reservation decisions made by the microprocessor are stored in a register and read out as needed in a 3-word reservation sequence.

The LICU transmits a polling address (the first word of the sequence) asking for reservation requests via the LI to all LIUs. (The polling address is generated by a modular 64 counter.) The polled LIU transmits reservation information to the LICU via the LI using the 2nd and the 3rd words: the 2nd word contains the destination address and the 3rd word contains the message length. The LICU stores the reservation information as well as the polling address in the reservation memory and then continues polling. The destination address is used to determine the memory status of the destination LIU to ensure its ability to receive a message. This determination is performed immediately prior to each transmission as part of the "front-end" handshake process.

After a preset number of reservations has been received, the LICU starts the transmission mode. Control data for transmission is prepared by the microprocessor and stored in registers to be gated out by the transmit enable signal. The first word in the transmit cycle is the polling address – now the address of the LIU which is to transmit data. If the destination memory is available, the LIU transmits it message on the LI, starting with the 2nd word after activation of the transmission enable signal. The destination LIU and the LICU detect the end of message word counts (obtained from the message by the LIU, and from the reservation information by the LICU). At the end of message, error checking is performed by the destination LIU. (The amount of time required for error checking is added to the transmission enable signal by the LICU.) The transmission enable is deactivated after each message transmission. The last word of the transmission enable period is the ACK/NACK from the destination LIU.

If the destination memory had not been available when a reservation is requested, the reservation is stored. The stored reservation is retried after the reservation memory completes a cycle.

A message transfer reservation from EIU is initialized by the EIU via a reservation request line, to provide a higher priority of LI access by the EIU. During the VB or LS cycle time, the reservation or message memory address counters and related functions of Block transfer are temporarily halted to provide priority for VB and LS transfer.

An LI interface capability is provided to exchange FI management control and configuration messages. Configuration messages are stored and transformed by the microprocessor to a suitable form for configuring the local timing. During initialization, the LICU transmits a prestored "active status" message to the FI manager to indicate ready to accept reconfiguration messages. Memory status reporting, timing generation and LICU initialization are described in the next topics.

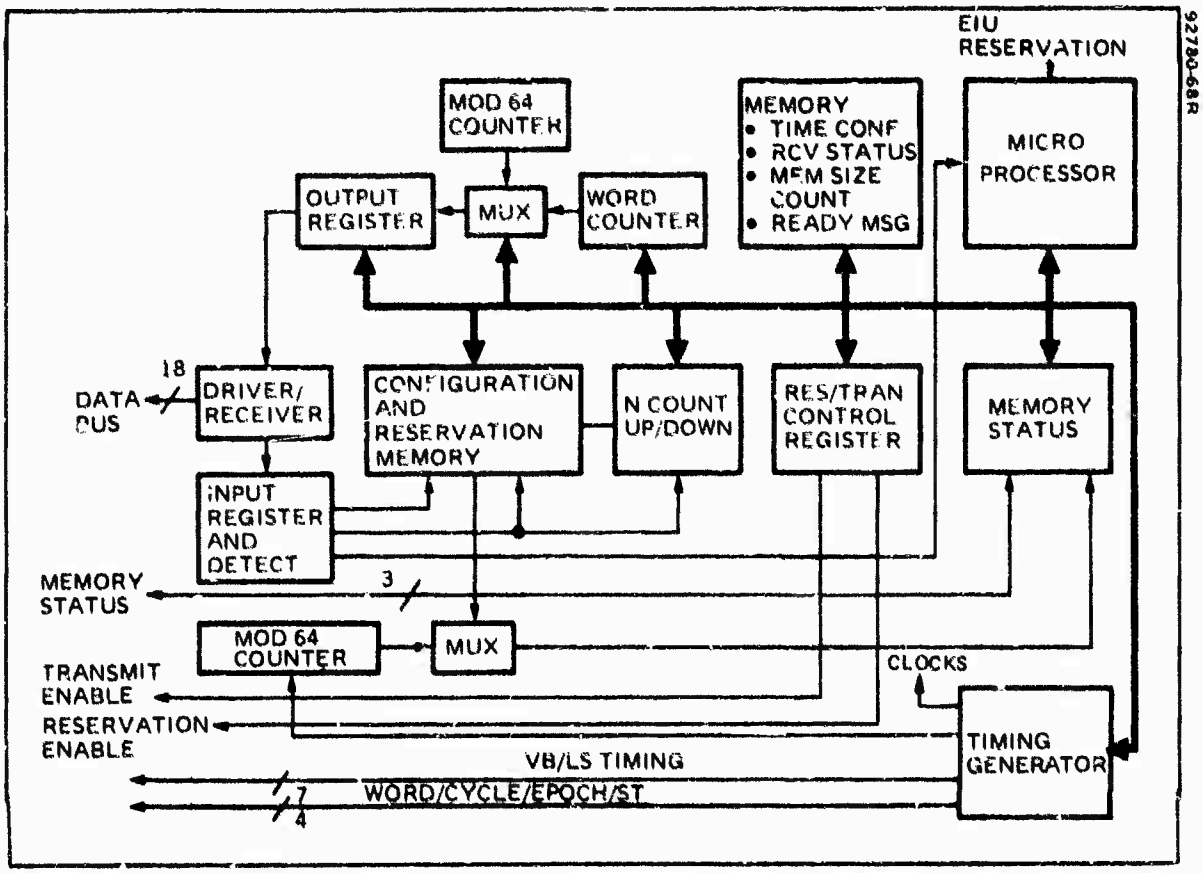


Figure 4.8.2-1. The LICU Functions. Local intraconnect control and timing functions for all LIUs are performed by the LICU.

3. MEMORY STATUS REPORT

Memory status reporting provides up-to-date information on destination memory availability. Bottleneck problems are thereby avoided and bus instability is prevented.

For discrete addressed message transfers, it is desirable to have prior knowledge of the destination receiver's ability to accept messages (receiver "memory status"), before transmission actually takes place. Messages would be lost if the destination receiver is unable to accept them and retransmission would be required. Retransmissions could potentially consume a large portion of the network capacity. This problem becomes more serious as traffic increases. If a device is a particularly active receiver, message losses increase resulting in even heavier message traffic loads due to retransmissions. This positive feedback situation could cause and aggravate bottleneck situations, resulting in instability.

In the FI, handshake methods are implemented to prevent these instability problems. Prior to each addressed message transmission, a front-end handshake procedure is carried out to assure that the message will be accepted by the addressed device. The front-end handshake is based on a memory status report from each LIU and EIU to the LICU. The LICU tabulates and tracks the "memory status" of the LIUs and EIU receiver local buffer memories. (Figure 4.8.3-1 depicts the timing of the memory status report.) Three unidirectional signal transfer lines constitute the memory status report mechanism. The LICU continuously generates a periodical signal called "memory status report cycle" to be transmitted to every LIU and the EIU. In each of the LIUs, the EIU and also the LICU, a modulo 64 counter is employed to provide the reporting sequence. The counter is reset by the "memory status report cycle" from the LICU, maintaining all counters in synchronism. The modulo 64 counter provides for a maximum of 63 LIUs and one EIU in each shelter. For each count, one of the LIUs or the EIU reports its local receive memory availability to the LICU. At a 5 MHz clock rate, 64 reports (63 LIUs and one EIU) requires 12.8 μsec. Therefor the LICU receives a memory update from all LIUs and the EIU every 12.8 μsec (memory status report cycle time). For each message transmitted, the LICU computes the memory size left at the destination device based on the summation of message lengths received by the device. The external memory status (each LIU has a separate receiver memory for messages from the EIU) is reported to the EIU from each LIU. It indicates the availability of the external memory section of each LIU for external message reception. The EIU computes the memory size which is left for additional message reception by each LIU based on the message lengths accumulated for each LIU. The amount of available external memory of each LIU is used in the front-end handshake decision process for external message transmission via the EI.

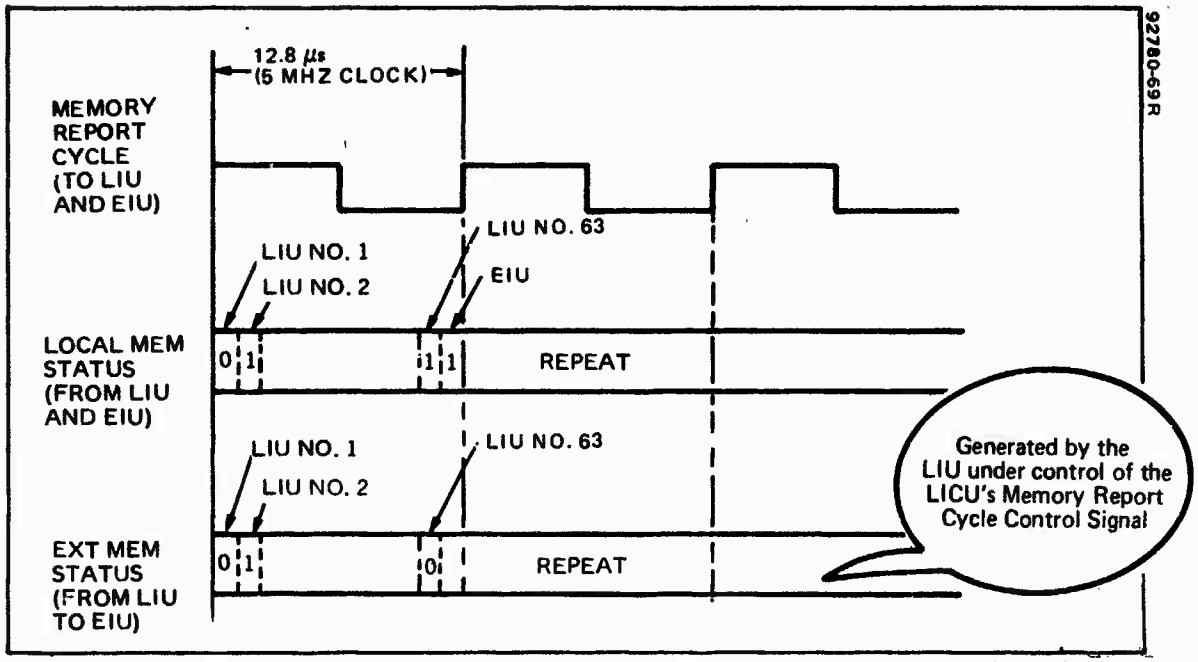


Figure 4.8.3-1. Front-End Handshake. Memory status lines indicate the status of the destination receive memories prior to transmission of messages.

4. IMPLEMENTATION OF THE LICU TIMING GENERATOR

The timing signals required for LI message transfer control are supplied by the LICU timing generator. The timing signals include clock pulses as well as control bus signals.

Timing is categorized into two groups: 1) basic timing, and 2) configuration timing. The basic timing function generates the word clock (5 MHz), the memory status report cycle, clock signals, System Time (1 MHz) clocks, and timing functions required for LICU internal processing. The word clock and memory report cycles are supplied to all LIUs and the EIU.

The programmable decoder generates all timing which varies according to data in the configuration memories (see Topic 8.4.5, LICU Initialization). The VB and LS control bus timing and the local cycle time must satisfy the configuration of VB and LS buses implemented in the FI and must meet the constraints set forth by the bus capacities and message lengths. These timing requirements are contained in the data stored in the LICU configuration and reconfiguration memories.

The implementation of the timing generator consists of a timing chain and timing decoding (shown in the diagram of Figure 4.8.4-1). The timing chain receives clock pulses from the clock source and counts down to obtain periodic signals at the required rates. The periodic signals are then used directly or are decoded further for the various functions. The clock source is 10 MHz. Standard counters implement many of the timing chain functions.

Both the basic timing decoder and configuration timing decoder use the outputs of the timing chain to generate desired timing signals. The basic decoding realized by Programmable Read Only Memories (PROMs) and the programmable decoding is realized by RAMs. The configuration timing decode function is determined by stored data. At startup configuration data comes from the basic configuration memory; after reconfiguration messages are received it comes from the reconfiguration memory. The stored configuration data is transformed by the microprocessor to form a suitable for programming the timing decoder. Configuration timing signals include VB/LS control bus timing, cycle timing and epoch timing. The LICU reservation control function also depends on outputs of the configuration timing decode function.

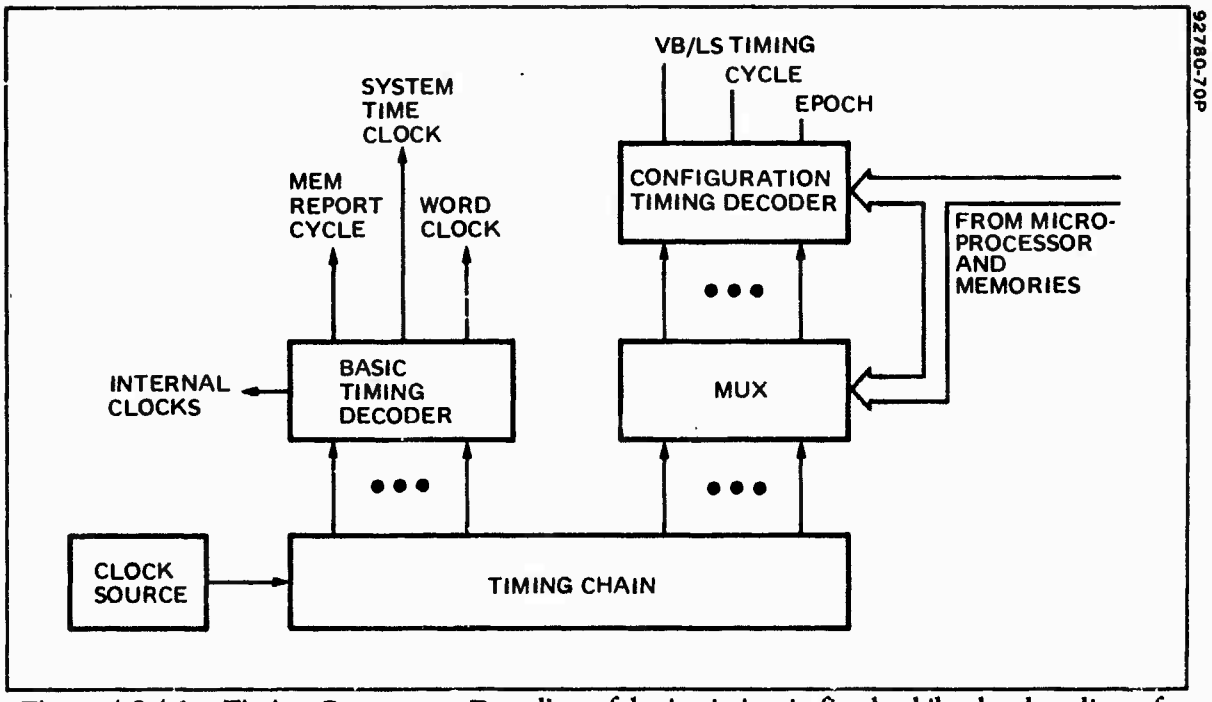


Figure 4.8.4-1. Timing Generator. Decoding of basic timing is fixed while the decoding of configuration timing is programmable.

5. LICU INITIALIZATION

Automatic initialization of the LICU allows rapid start-up and operation of the Local Intraconnect.

Storing parameters which determine the operating configuration of the LI is one of the key functions of the LICU. These parameters allow it to control the operation of the LI at start-up and thereafter without depending on an outside FI management function.

A non-volatile store of basic configuration data is designed into every LICU. The basic configuration, discussed in more detail in the FI management section of this report (see Part 4, Section 10) consists of a mix of Block, VB and LS message transfer capabilities. This mix is the same in all LICUs. The LICU also stores reconfiguration data when received from the FI management function. The LICU timing generation function, the Block message reservation control function, and the VB/LS control bus operation are all based on configuration data.

After power is applied to the LICU it automatically begins operating according to the basic configuration stored in its basic configuration memory (see Figure 4.8.5-1). The first message transmitted on the LI by the LICU is its own active status message to any existing FI Management function (the contents of active status messages are also described in Section 10, FI Management). The active status message announces the existence of this LICU and indicates that it is ready for any reconfiguration messages. If there is no active FI Management function, no configuration messages will be received and operation will continue in the basic configuration (as will all other elements of the FI). Periodically, as long as the LICU is operating, it sends an active status message. The period is determined by an internal LICU counter.

If a configuration message is received, it is stored in the reconfiguration memory. From then on, unless it is redirected by the FI Manager or loses power and stops operating, the LICU controls LI operations based on the contents of its reconfiguration memory.

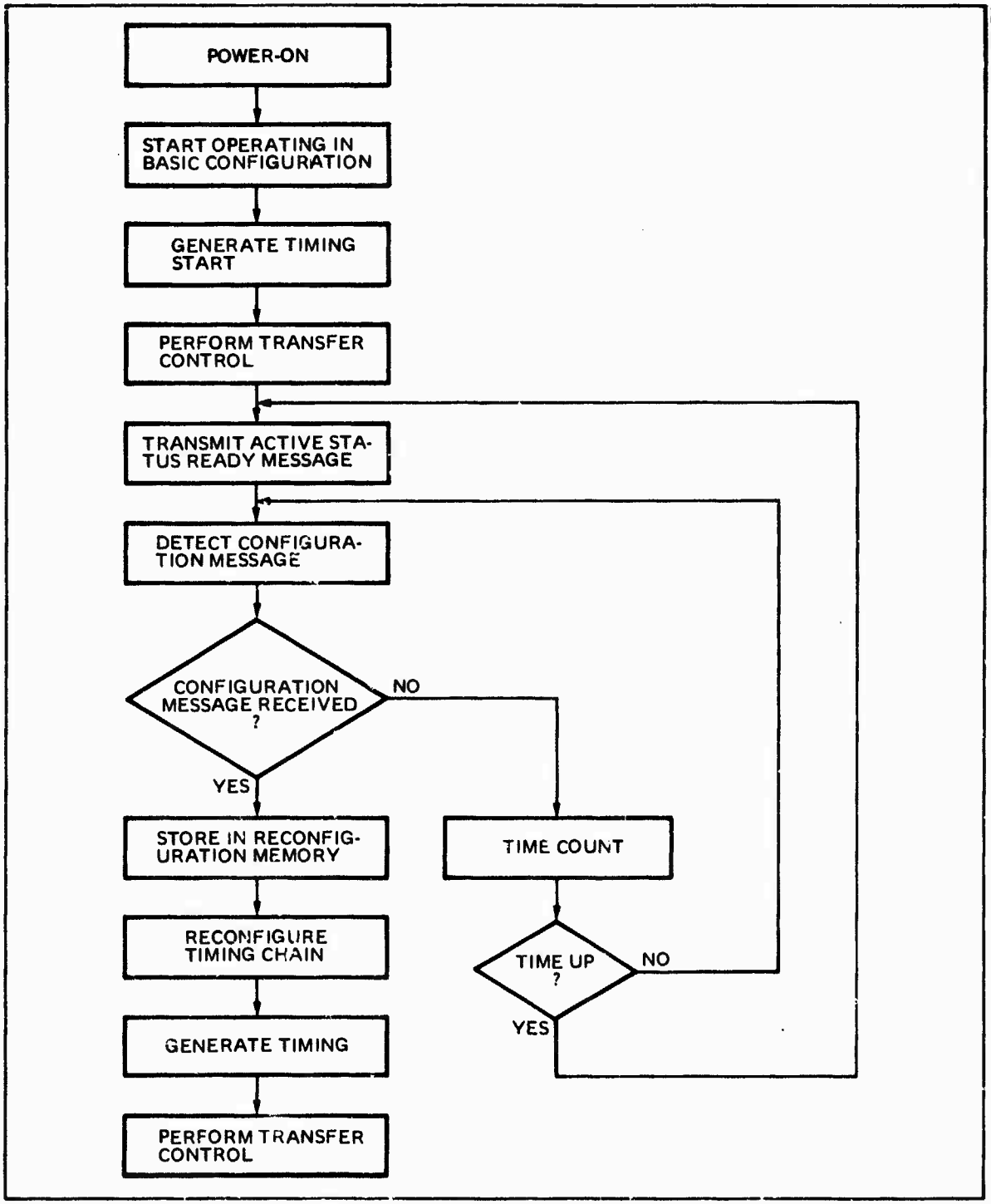


Figure 4.8.5-1. LICU Initialization Sequence. The LICU initialization procedure automatically starts operation in the basic configuration. Reconfiguration messages from the FI Manager modify LICU operation.

SECTION 9
UNDETECTED ERROR RATE ANALYSIS

Part 4 – Task III, Preliminary Design Analysis
Section 9 – Undetected Error Rate Analysis

1. SUMMARY OF THE UNDETECTED ERROR RATE ANALYSIS

The undetected error rate analysis shows that the FI design meets or exceeds the required rates.

Since the ideal goal of moving data from a source to a destination without error is not possible, the practical goal is to transfer data with an integrity that is acceptable to the user. This usually becomes a compromise between the cost of ensuring a high degree of data integrity and the cost of an error times the error rate during the lifetime of the transmission system.

The requirement as specified in Draft Military Standard MIL-STD-XXX, 1 January 1979, is for an undetected error rate of one bit in 10^{12} bits in the transmission of data and no more than one undetected header error in 5000 years assuming a header transmission rate of 5000 per second.

The FI has two basic transmission paths: intrashelter and intershelter. Figure 4.9.1-1 shows the data path for both situations. In the case of intrashelter operation, both the source and destination DTEs connect through a single LI link. Only the intershelter operation requires the use of EI links.

The error control starts at the point in a transmitting DTE where the error detection bits are added to the data. Error Control ends in the receiving DTE(s) where error control interpretation occurs. As per Government direction this error analysis includes only those elements which effect the bus structure, i.e., the memory and drivers in the LIUs and EIUs and the LI and EI links.

The required error rate (5000 headers per second for 5000 years) equates to an undetected Header error rate of 7.884×10^{-14}. The computer intershelter undetected header error rate for the Hughes design is about 1.78×10^{-14} for eight shelters.* The undetected data bit error rate is specified to be better than 10^{-12}. Using the intershelter configuration in the worst case configuration for eight shelters, the computed undetected data bit error rate is 0.832×10^{-12}.

Intershelter data must traverse the transmit EI links to the last EIU, loop around to the receive EI links, and continue to the receive EIU. As a result, the intershelter undetected error notes are a function of the number of EI links in the path from source to destination.

Figure 4.9.1-2 and 4.9.1-3 graphically represent the undetected error rates for the header and data, respectively. It can be seen that the data undetected error rates exceeds the specified maximum when the number of EI links exceeds 98 (i.e. 50 shelters).

The detailed explanations of the error sources and the Undetected Error Rate analysis calculations are presented in the following topics.

*The computations used to arrive at these error rates are presented in Topic 4.9.3.

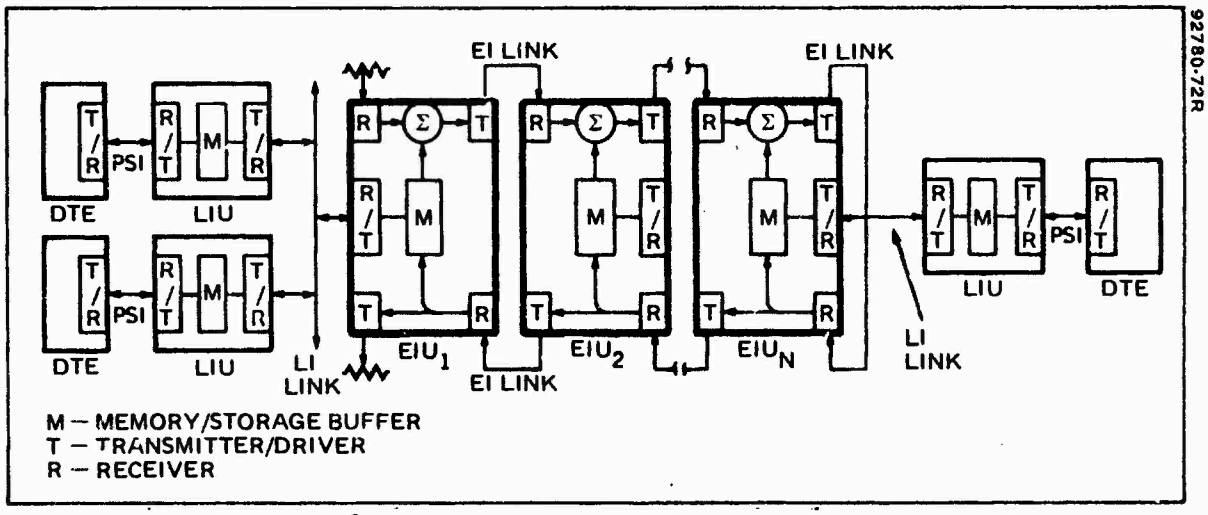


Figure 4.9.1-1. Modular C^3 Transmission Diagram. The intrashelter configuration consists of LIUs on one LI link only. The intershelter configuration uses the EIUs and EI links as well.

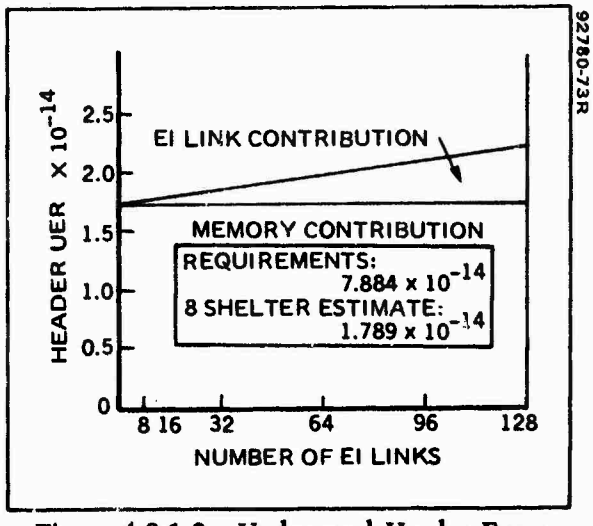


Figure 4.9.1-2. Undetected Header Error Rate vs Number of EI Links

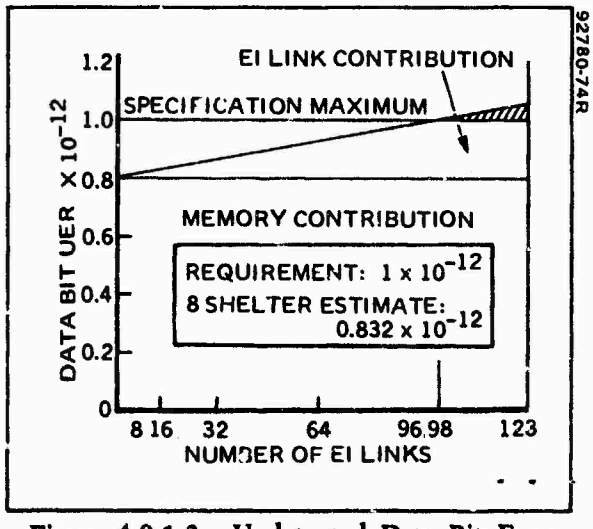


Figure 4.9.1-3. Undetected Data Bit Error Rate vs Number of EI Links

2. ERROR CONTROL MECHANISMS

The method for determining the undetected error rate is a function of both the error detection technique and the data configuration. The header and data portions of a message have different criteria.

The wide variety DTEs which may be interconnected via the FI can cause problems in relation to any error control mechanisms which may be employed. While the headers have a defined parity word the variation in DTE types precludes depending on DTE error control for the data.

The header consists of sixteen words, each containing eighteen bits. The last word is a longitudinal parity check on the previous fifteen words. (Figure 4.9.2-1 represents the header configuration.) The probability of error of a bit in each one of the sixteen words is $16 \times P_E$, where P_E is the bit error rate. An undetected error occurs if an even number of bits are in error. The probability of a second bit in error is $15 \times P_E$. The probability that the two errors will occur in one longitudinal row in a header is:

$$= 16 \times P_E \times 15 \times P_E = 2.4 \times 10^2 \times P_E^2$$

In considering the entire header (18 bits per word), then:

$2.4 \times 10^2 \times 18 \times P_E^2 = 4.32 \times 10^3 \times P_E^2$ = undetected header error rate.

Other even numbers of errors would also cause an undetected error. These occurrences are less likely (by many orders of magnitude) and can be ignored.

The data portion of the message is of variable length up to maximum of one thousand words. It is assumed that this data is transparent to the FI. For this analysis it is assumed that the eighteen-bit words will not be modified. Two approaches may be implemented: adding a nineteenth bit for parity to each word (word parity) or, using longitudinal parity at the end of the data.

If the word parity technique, as shown in Figure 4.9.2-2, is used, the undetected bit error is:

$$19 \times P_E \times 18 \times P_E = 3.42 \times 10^2 \times P_E^2$$

The longitudinal parity approach requires the use of five parity words operating on the data message bits in an interleaved fashion as shown in Figure 4.9.2-3. The probability of error is:

$$P_0 + \sum_{n=0}^{m} b_{5n} = 1$$

$$P_1 + \sum_{n=0}^{m+1} b_{1+5n} = 1$$

$$\bullet$$
$$\bullet$$
$$\bullet$$

$m + 4 \leq$ last data word

$$P_4 + \sum_{n=0}^{m+4} b_{4+5n} = 1$$

The worst case (assuming 1000 word maximum data length) would be:

$$201 \times P_E \times 200 \times P_E \times 5 \text{ for 1000 words}$$

$$= 2.01 \times 10^5 \times P_E^{\,2} = \text{data undetected bit error rate}$$

The longitudinal parity implementation was selected because of the lower bit count per message since the error rate derived from this implementation meets the requirements.

B_1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	P
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	P
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	P
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	P
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	P
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	P
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	P
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	P
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	P
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	P
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	P
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	P
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	P
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	P
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	P
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	P
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	P
B_{18}	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	P
	W_1	W_2	W_3	W_4	W_5	W_6	W_7	W_8	W_9	W_{10}	W_{11}	W_{12}	W_{13}	W_{14}	W_{15}	

92780-75R

Figure 4.9.2-1. Header Parity Implementation

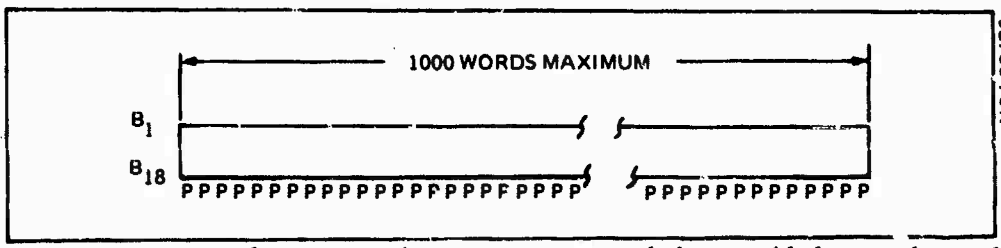


Figure 4.9.2-2. Word Parity Implementation. A 19th bit is added to each word.

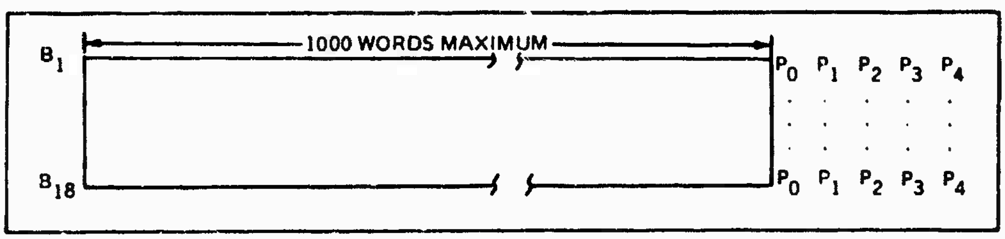


Figure 4.9.2-3. Longitudinal Parity Implementation. This technique adds 90 bits to the message.

3. UNDETECTED ERROR RATE CALCULATIONS

The sources and causes of errors in the transmission path are functions of the devices and speeds used. Statistical data on each identifiable part of the data is available or estimatable. Before an undetected error rate can be determined, the error rates for each element must be known.

The memory (buffer) and error control logic has an error rate of 10^{-9}. This is for C-MOS and is the worst case situation. Other technologies provide better error rates. Empirical data indicates that a point-to-point fiberoptic link for the lengths considered, including the driver and receiver, has an error rate in the order of 10^{-10}. The LI link is assumed to have an error rate of 10^{-11}.

These undetected error rates (UER) must be considered with respect to the data flow and the resultant error exposure windows that exist. Table 4.9.3-1 shows that the intrashelter data path consists of two memories and the LI link. The intershelter data path requires 2 LIU, 4 memories (1 in each LIU and the terminating EIUs) and a number of EI links. The number of EI links depends on the locations of the originating and terminating DTEs.

The calculations for the intrashelter operation are shown in Table 4.9.3-1. It should be noted that the calculations are separate for the header and the data.

In considering the intershelter operation, the number of EI links is important. The calculations shown in Table 4.9.3-2 are based on a hypothetical center using eight shelters. The worst case is shelter one sending to shelter two since it requires the most EI links. The number of EI links is fourteen.

It was noted during this evaluation that the memory causes the major impact on the undetected error rate. Table 4.9.3-3 gives the UER's for a range of EI links. These can be compared to the memory and LI link UERs at the bottom of the table.

TABLE 4.9.3-1. UNDETECTED ERROR RATES FOR INTRASHELTER OPERATION

HEADER		
2 Memories	$2 \times 4.32 \times 10^{3} \times 10^{-18}$	
1 LI Link	$4.32 \times 10^{3} \times 10^{-22}$	
	8.64×10^{-15}	= Header UER
DATA		
2 Memories	$2 \times 2.01 \times 10^{-5} \times 10^{-18}$	
1 LI Link	$2.01 \times 10^{5} \times 10^{-22}$	
	4.02×10^{-13}	= Data UER

TABLE 4.9.3-2. UNDETECTED ERROR RATES FOR INTERSHELTER OPERATION FOR EIGHT SHELTERS, SHELTER ONE TO SHELTER TWO

HEADER

4 Memories	$4 \times 4.32 \times 10^{3} \times 10^{-18}$
2 LI's	$2 \times 4.32 \times 10^{3} \times 10^{-22}$
14 EI's	$14 \times 4.32 \times 10^{3} \times 10^{-20}$
	1.7886×10^{-14} = Header UER

DATA

4 Memories	$4 \times 2.01 \times 10^{5} \times 10^{-18}$
2 LI's	$2 \times 2.01 \times 10^{5} \times 10^{-22}$
14 EI's	$14 \times 2.01 \times 10^{5} \times 10^{-22}$
	0.832×10^{-12} = Data UER

TABLE 4.9.3-3. UER RANGE VS. EI LINKS

# of EI Links	Header UER's ($\times 10^{-14}$)	Data UER's ($\times 10^{-12}$)
2	1.7367	0.808
4	1.7454	0.812
8	1.7626	0.820
14	1.7886	0.832
16	1.7972	0.836
32	1.8663	0.868
64	2.0046	0.937
126	2.2724	1.057
4 Memories	1,728	0.804
2 LI Links	0.00008	0.00004

The UER for the 4 memories and 2 LI links is 1.72808×10^{-14} for the Headers and 0.80404×10^{-12} for the data. It should be noted that the memories are the main source of errors.

SECTION 10
FI MANAGEMENT

1. KEY FEATURES OF FI MANAGEMENT IMPLEMENTATION

FI flexibility results from an approach in which FI management is partitioned from FI control, with command and response messages providing the bridge between the two functions.

Basic start-up and control functions are implemented in FI elements, providing the ability within the FI to activate itself and operate with a basic capability and configuration, and without the need for an FI management function. However, the FI is also designed so that an FI management capability, implemented in the hardware and/or software of data terminal equipment (DTE), can reconfigure the FI with different configurations. FI monitoring, test functions, and other special services can also be performed by FI management. These FI management functions can be distributed among DTE elements, giving C^3 Centers the flexibility necessary for rolling force or leap frog tactics and increasing system survivability.

Basic control of each Local Intraconnect, resides in the local intraconnect control unit (LICU). Basic control of the External Intraconnect is shared between External Intraconnect Units (EIU) in the shelters. Each Local Intraconnect Unit (LIU) contains some of the logic for controlling transfers on the FI. The FI units contain all the control functions necessary for operating the flexible intraconnect and also contain all the storage mechanisms for storing current FI configuration data.

FI management functions are implemented outside of the flexible intraconnect in DTEs, and as an example could exist as illustrated in the shaded portions of Figure 4.10.1-1. The FI management function can be implemented in a single processor or can be distributed among various user equipments such as CPU smart displays, in peripherals, or via operator manual input devices. FI management functions can be distributed among DTEs in many shelters, as well. The key vehicle allowing this flexible distributed management function to work is command and response messages. These communicate the directions of the FI Manager to the FI control functions and carry status and requests to and between FI management functions. Within this scheme of FI management the level of sophistication of the FI management function can vary from the simplest basic configuration, to complex levels under hardware and software control of user DTEs. FI management is limited strictly to the flexible intraconnect as a network, and does not apply directly to operation, management, or control of DTEs.

The separation of FI control function implementation from FI management function implementation is important in another aspect. FI operation does not depend on continuation of FI management services. That is, not only can the FI operate with its basic control functions after start-up, but should FI management services exist and subsequently be lost, FI operation will continue with its most recent configuration in effect. The FI operating within a command control center can be initiated and operated in the field by personnel with a minimum of training. Sophisticated re-configurations can be achieved via prerecorded devices or by cook book style manual inputs.

The roles of FI management which include (1) activation/deactivation management, (2) configuration management, (3) FI monitoring and test, and (4) special services, are described in more detail in the next topics.

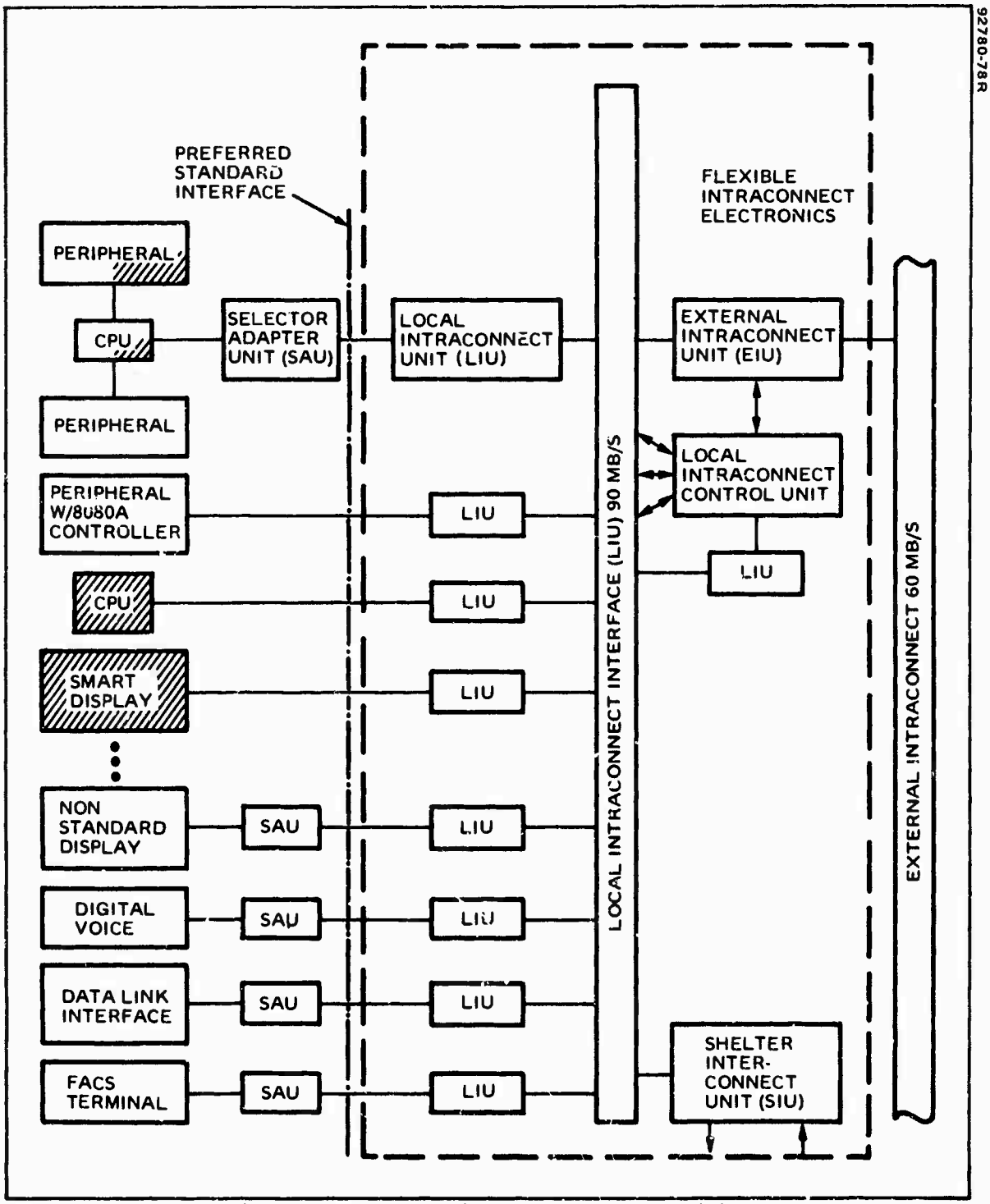


Figure 4.10.1-1. Typical FI Management Implementation. FI control functions exist within the flexible intraconnect but FI management is implemented in DTE's. (Examples of potential FI Management residence are shaded).

2. ACTIVATION/DEACTIVATION MANAGEMENT

Independent and automatic activation/deactivation of each FI element permits basic operations to proceed without an FI management function, and also permits FI management, when it exists, to manage the scope of operations and the system configuration.

Basic activation/deactivation control of elements within the flexible intraconnect is inherent in the design of each of the elements. When power is applied to the elements of the flexible intraconnect, those elements become active operating in a basic configuration. (See Figure 4.10.2-1). Without an FI management function operation continues indefinitely in this configuration, as explained in the next topic. While in this basic configuration any new elements may become active on the FI in the same way as the original elements. Should an FI management function exist, having implemented an other than basic configuration, newly activated FI elements will be recognized by the FI management function via automatic status messages, and will be sent appropriate configuration data via command messages. Deactivation of units may occur independently and automatically (e.g. at power off). The FI management function has the ability to control active participation on the FI via authorization codes sent to each LIU. It also has the ability to deactivate units via deactivation command messages.

The basic configuration includes the ability to distribute command and response messages and to communicate directly with an FI Manager. This permits active status messages to announce the existence of each FI member so that the FI Manager may subsequently exercise reconfiguration and FI activation/deactivation management.

The initialization or activation process for a newly started LIU is a simple procedure. Upon entering an operational FI, an LIU notifies any existing FI management function of his presence with an active status message. If a configuration different from the basic FI configuration has been implemented by the FI Manager, the FI Manager will automatically transmit reconfiguration information to that LIU, including authorization codes, virtual address data, Virtual Bus and Lazy Susan data. Operation of the newly started LIU proceeds according to the then-current FI configuration.

The EIUs are the only FI elements which require a manual input prior to effective operation. Since EIU operating addresses cannot be predetermined for all configurations, an operating address must be loaded into each EIU prior to effective operation. The EIU address number is set into an EIU via switches on the EIU. Once these are properly set, an EIU starts operations in a manner similar to that described for an LIU.

LICUs activate automatically with the application of power, first transmitting active status messages to the FI Manager and then proceeding to operate in the basic configuration, permanently stored in their configuration maps. When reconfiguration information is received from the FI Manager, the LICU modifies its operation accordingly.

The FI management function has the ability to over-ride individual active/status functions of each FI element via authorization codes and deactivate command messages. This management function may be used as part of FI management reconfiguration operations, activating elements for backup deactivating elements that are malfunctioning or orchestrating the complement and functions of a C^3 center for survivability, buildup, scaledown or graceful degradation.

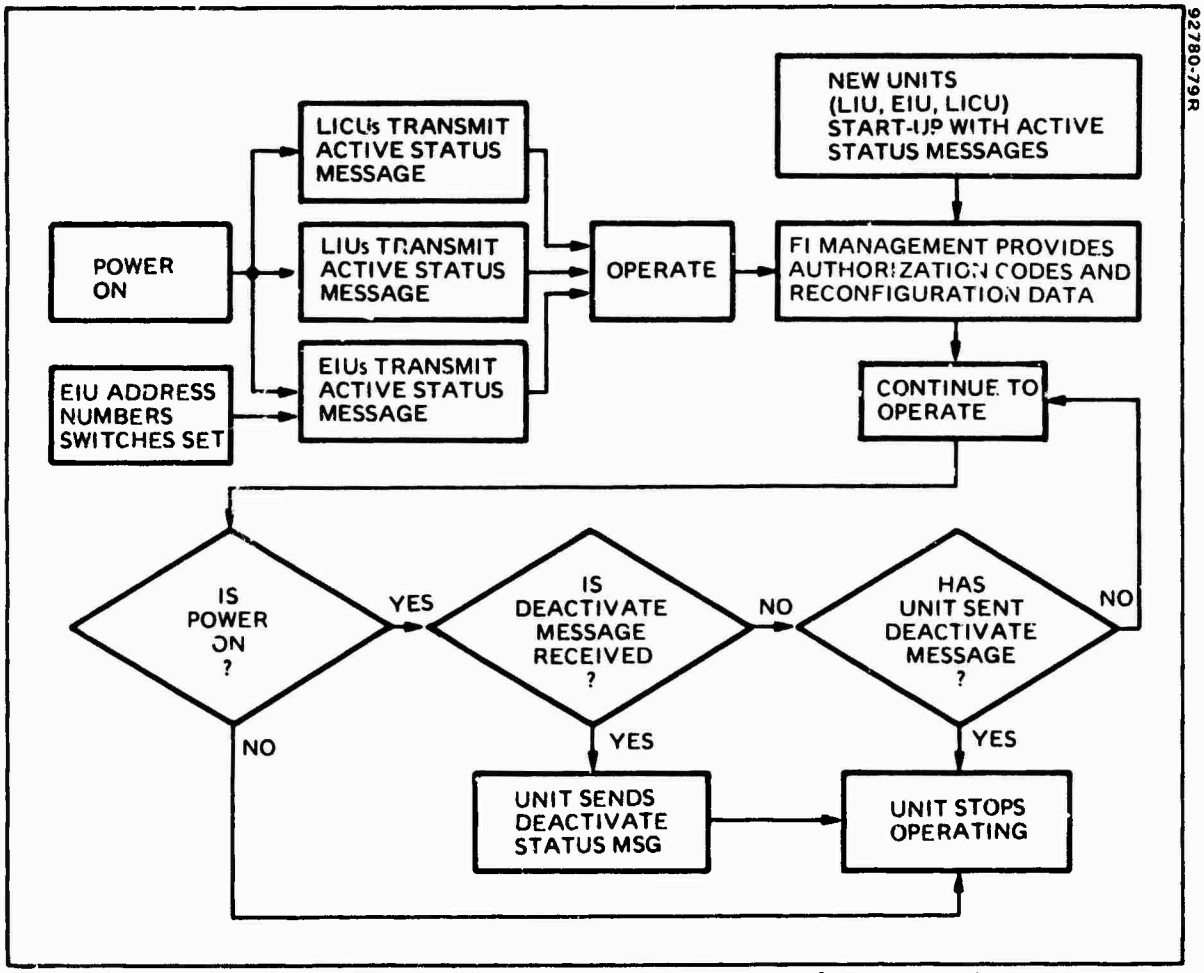


Figure 4.10.2-1. Activation/Deactivation Functions. Activation of FI units and FI operation is automatic but the FI Manager maintains configuration authority via authorization codes, configuration and deactivation command messages.

3. FLEXIBILITY THROUGH MANAGEMENT OF FI CONFIGURATION

FI Management implements reconfigurations via command messages which provide modifications to on-line configuration maps and tables stored in LIUs, LICUs and EIUs.

Consistent with the philosophy of the FI management concept, control of an established configuration is implemented within the FI, but FI reconfiguration is implemented from DTEs operating in an FI management role (see Figure 4.10.3-1). For purposes of this discussion, FI configuration includes the complement and status of FI units operating within a center, the types and modes of operation of these units (authorization codes, message types, modes, DTE types), their operating real and virtual addresses, and the timing structures of the external and local intraconnects (reservation slots, Short Block and Block message slots, Virtual Bus slots, and Lazy Susan slots).

Real-time, on-line configuration control in each shelter, is resident in the local intraconnect control unit (LICU) where configuration maps are stored and the local timing structure is controlled. Message type, mode, virtual/read address and authorization code control exists within each local intraconnect unit (LIU); external intraconnect timing structure control resides in the external intraconnect units (EIU). These units store the current FI configuration in their memories and operate accordingly. FI management may then designate, process, and calculate the requirements and parameters for new or changed FI configurations, and send appropriate deletions and additions to the FI units via configuration command messages.

Basic FI configuration data is permanently stored in each of the units of the FI, so that the FI may start up and control itself without the need for an FI management function. Although an FI management may then designate, process, reconfigure the FI to suit its needs, the basic FI configuration includes the capabilities, not only to respond to FI management, but to serve the message and data distribution needs of small or simple centers, where no FI management function is implemented. All FI management functions implemented in DTEs will operate with a fixed predetermined reserved address, allowing newly activated units to address FI management without having to be specifically configured. Included in all basic configurations is the capability for exchanging command and response messages to permit any FI unit to communicate with the FI management function if it exists. A Block message system accommodates command and response messages, discrete addressed messages and broadcast messages. A select number of limited bandwidth Virtual Bus and Lazy Susan channels are also included in the basic configruation to accommodate common requirements of most small centers (for example, voice communications or data base sharing). All FIs will have the basic configuration "built-in", and all potential users may depend on that configuration, even without implementing an FI management function in one or more of the DTEs.

In order to perform the configuration management role, FI management must be able to receive manual or prerecorded inputs or messages which describe reconfiguration requirements. It must also be able to transmit, receive and process command and response messages. The processing involved in translating reconfiguration requests and requirements, to parametric data, need not be performed on line. Because of the separation and indeperdence of FI control functions from FI management functions, the configuration management processing can be performed off-line with the results communicated to units via on-line command and response messages.

The calculation of Sequence Number assignments for units operating within a Virtual Bus or Lazy Susan network is not normally a function of FI configuration management, but may be performed as a special service of FI management (described in Topic 4.10.5).

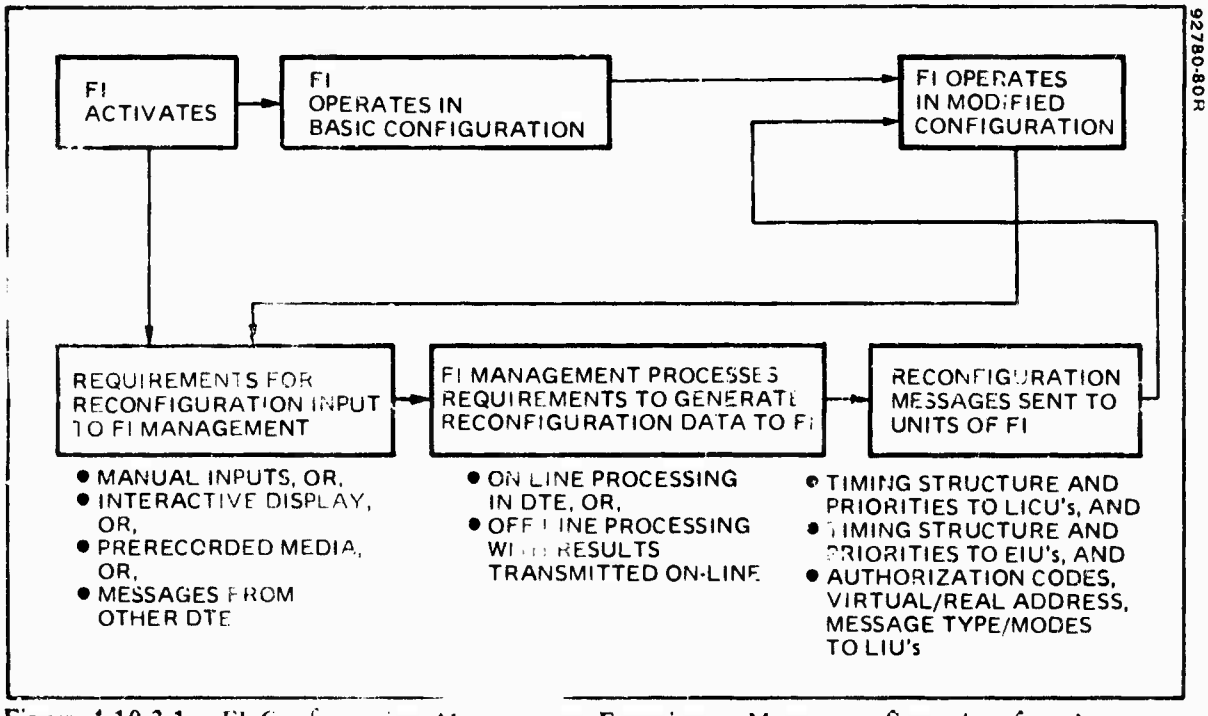


Figure 4.10.3-1. FI Configuration Management Functions. Most reconfiguration functions may be performed off-line, but reconfiguration messages are transmitted on-line.

TABLE 4.10.4-1. FI MONITORING MODES.

PASSIVE MONITORING VIA DESIGNED-IN AUTOMATIC REPORTING
• Status Messages
• Error Messages
ACTIVE MONITORING BY INTERROGATION
• Status
• Configuration Data
• Table Contents
• Counter States
• Test Messages

5. SPECIAL SERVICES OF FI MANAGEMENT

The FI management function enhances C^3 operation by using its off-line processing functions to assist unsophisticated user devices with header construction.

In addition to the normal services of FI management there are special services that can be performed by FI management to aid user DTEs. These services include the preparation of "prefix headers" for simple, less sophisticated users and sequence number/metering rate calculations for Virtual Bus and Lazy Susan users (see Table 4.10.5-1).

While most DTEs operating with the FI will have total capability to operate with the Preferred Standard Interface, some users may need help in preparing and constructing headers for messages. Headers, normally prepared by the DTE or a Selected Adapter Unit (SAU), can be prepared and supplied to the appropriate LIU by FI management. This "prefix header" preparation is practical for DTEs that transmit messages to only one address for long periods of time. For example, a peripheral equipment DTE (such as a magnetic tape unit, or a keyboard entry device) may have an interface controller which is capable of performing simple word and block transfer control at the PSI, but may not have the processing capability to prepare its own message header. Since such a DTE would be sending all of its data to one device (for example a host CPU) a "prefix header" could be prepared for it by FI management. A typical operational scenario for such a case would have the request and parametric requirements for the "prefix header" including destination and source address, message type, and mode, presented to the FI management function via manual inputs. FI management processing would prepare a full 16 word "prefix header" and send it to the appropriate LIU via a command message. Subsequently the LIU would fill in dynamic header words such as message number, and attach the "prefix header" to all messages transmitted on the FI by the DTE. Should operational requirements make it desirable, FI management could periodically (not dynamically) prepare a new header (perhaps with a new destination address) for the same LIU/DTE, permitting it to service a different host or to utilize a different FI transfer system.

Virtual Bus and Lazy Susan message transfer systems operate as capabilities within the FI, but are individually controlled by their DTE users. For example, a Virtual Bus may be included in the FI configuration with a designated bit rate capacity, and with Virtual Bus management authority designated to a particular DTE user (via authorization codes provided to its LIU). Normally, that DTE would calculate or provide transmission Sequence Number assignments to each of the intended users of the Virtual Bus, according to the desired transmitting order and metering rate. Since some potential users of Virtual Buses and Lazy Susans may not have the capability to calculate Sequence Number assignments appropriately, that service is provided by FI management special services. A typical scenario which involves this special service might proceed as follows. A Virtual Bus is included in the FI configuration with one megabit per second

capacity, and with a particular CPU as the Virtual Bus manager. The CPU may (as a result of its own manual inputs, or otherwise) send a request message to the FI management function designating a family of users of the Virtual Bus, the metering rate for each user and the preferred order of transmission. The FI management function will then calculate and assign appropriate Sequence Numbers and Virtual Bus transmission authorization codes to the LIUs of the Virtual Bus user family. Operation of the Virtual Bus may then proceed. Lazy Susan Sequence Number calculation services would follow a similar scenario even though the Sequence Number calculation algorithm is different.

"Prefix header", Virtual Bus and Lazy Susan special services are another feature of FI Management which enhances the flexibility of C^3 Centers operating with an FI.

TABLE 4.10.5-1. FI MANAGEMENT SPECIAL SERVICES

Prefix header construction for unsophisticated devices

- Manual inputs sets fixed header parameters
- FI management constructs 16 word prefix header
- Prefix header sent to LIU via command message
- LIU adds dynamic data to header and attaches prefix header to data portion of each message prior to transmission

Virtual Bus and Lazy Susan services

- Request for service to FI management including:
  - VB/LS number
  - User addresses
  - Transmission sequence order
  - Metering rates
- FI management calculates Sequence Number structure and assignments
- FI management sends Sequence Number assignments and authorization codes to appropriate LIUs

SECTION 11
RELIABILITY

1. ESTIMATE OF CURRENT AND PROJECTED FI UNIT RELIABILITY

Current MTBF estimates for the individual FI units range from 18,000 to 32,000 hours. This can be expected to improve to 67,000 to 93,000 hours per unit in five years.

A reliability analysis was conducted to assess the potential inherent reliability of the FI. Since the configuration of the FI is system dependent, the basic analysis was conducted at the unit level and not the system level. Additionally, the analysis examined the inherent unit reliabilities which could be obtained using current available standard components, and the projected reliability postulated on the basis of standard components expected to be availavailable in five years.

The results of the reliability analysis are presented in the tables. Table 4.11.1-1 presents the current reliability estimates and Tables 4.11.1-2 presents the projected estimates. The estimated mean time between failures (MTBF) for the FI units, if produced today, are 18,700 hours for the LIU, 32,100 hours for the LICU, and 18,000 hours for the EIU. Corresponding five-year projections are 67,000 hours for the LIU, 93,000 hours for the LICU, and 88,000 hours for the EIU.

The predicted reliability is based on preliminary design data interpreted in terms of the quantity of parts (generically) and circuit cards per unit. The estimated generic part counts are indicated in the facing tables for each of the FI unit types. Generic component failure rates are derived from MIL-HDBK-217B (Notice 2) for fixed ground operation and 35°C ambient air flow over the parts. These conditions are typical for a fixed operating site or sheiterized system configuration with equipment cooling using air conditioners.

The difference in current and projected failure rates is primarily due to the quality level assumed for the integrated circuits. The present day prediction assumes full JAN-B (MIL-M-38510/Class B) quality for SSI, linear, and 4k RAM devices. The microprocessors, LSI, 16k RAM, and 16K ROM devices are assumed to be vendor equivalent B level quality (B-2). For the projected reliability prediction, it is assumed that full JAN - B devices would be available for all ICs. The complexity of the ICs is taken to be 20 equivalent gates for each SSI/MSI, 300 gates for the LSI, and 1350 gates for the 8-bit RCA 1802 microprocessor.

The PIN Diode failure rate is based on accelerated test data on the TI L-81 photo transistor. This data is based on 125°C operation and considered extremely pessimistic. Projected failure rates are based on the reliability of a single JANTX transistor.

The largest failure rate contributor for all units is the 16k RAM. This is due to the high complexity of the device, the relative immaturity of the devices, and the limited amount of operational failure data available. It is expected that as more of these devices are used, and their maturity improves, a dramatic reduction in their failure rate will be observed (as was the case for 1k and 4k RAMs when they were first introduced).

TABLE 4.11.1-1. CURRENT FI RELIABILITY

COMPONENT TYPE	COMPONENT FAILURE RATE *	LIU		LICU		EIU	
		QTY.	FAILURE RATE	QTY.	FAILURE RATE	QTY.	FAILURE RATE
MICROPROCESSORS (8 BIT)	2.31	1	2.31	1	2.31	1	2.31
SSI/MSI	0.03	102	3.06	76	2.28	2	0.06
LSI	0.82	3	2.46	3	2.46	3	2.46
RAM (16K)	3.89	10	38.90	5	19.45	6	23.34
RAM (4K)	0.33	-	-	4	1.32	-	-
ROM (16K)	1.12	2	2.24	-	-	3	3.36
LED	0.04	-	-	-	-	3	0.12
PIN DIODES	5.71	-	-	-	-	3	17.13
LINEARS	0.03	-	-	-	-	12	0.36
CONNECTORS	0.45	4	1.80	4	1.80	8	3.60
5% FOR PASSIVE	-		2.54		1.48		2.64
TOTAL FAILURE RATE *			53.31		31.10		55.38
MTBF (HOURS)			18,758		32.154		18,057

*Failure rate expressed in failures per 10^6 hours.

TABLE 4.11.1-2. PROJECTED FI RELIABILITY

COMPONENT TYPE	COMPONENT FAILURE RATE *	LIU		LICU		EIU	
		QTY.	FAILURE RATE	QTY.	FAILURE RATE	QTY.	FAILURE RATE
MICROPROCESSORS (8 BIT)	0.46	1	0.46	1	0.46	1	0.46
SSI/MSI	0.03	102	3.06	76	2.28	2	0.06
LSI	0.16	3	0.48	3	0.48	3	0.48
RAM (16K)	0.78	10	7.80	5	3.90	6	4.68
RAM (4K)	0.33	-	-	4	1.32	-	-
ROM (16K)	0.22	2	0.44	-	-	3	0.66
LED	0.04	-	-	-	-	3	0.12
PIN DIODES	0.10	-	-	-	-	3	0.30
LINEARS	0.03	-	-	-	-	12	0.36
CONNECTORS	0.45	4	1.80	4	1.8	8	3.60
5% FOR PASSIVE	-		.70		.51		.54
TOTAL FAILURE RATE			14.74		10.75		11.26
MTBF (HOURS)			67,842		93,023		88,809

*Failure rate expressed in failures per 10^6 hours.

2. PROJECTED FI SYSTEM RELIABILITY

The projected MTBF of a single shelter FI is about 20,000 hours in a typical system configuration which assumes that no single interfacing equipment failure will result in a shelter failure.

The functional block diagram for a single shelter FI (Figure 4.11.2-1) and a reliability block diagram for a hypothetical FI system configuration, are shown on the facing page. The reliability block diagram (Figure 4.11.2-2) for a single shelter FI is one branch of the system reliability block diagram.

Since the shelter FI configuration is system dependent (i.e., determined by the number of devices), a fixed FI reliability assessment cannot be established at the shelter level. Assuming that the typical system into which the FI will be integrated contains physical and functional redundancies the loss of any single device will not result in a system (shelter) failure. Likewise, the loss of a single LIU will only prevent communicating with a single device and will not result in a shelter failure. Therefore, if the FI is designed to permit on-line replacement of LIU circuit cards, it can be modeled (for reliability purposes) as having redundant LIUs (i.e., if N LIUs are used, only N-1 are required to be operational). With this assumption, the FI reliability model reduces to a serial string of the LICU, EIU, and miscellaneous hardware elements (i.e., λ LIU (effective $\cong$ 0). The resulting effective MTBF of the FI is in excess of 23,000 hours.

The above reliability estimate, based on projected failure rates described in the preceding topic, can be increased even further through reliability directed design. Redundant power supplies are an easy way of improving the FI MTBF while redundant EIUs (or portions thereof) or redundant LICUs can add reliability but at a higher design cost. With these improvements the inherent reliability could be 100,000 hours or more.

From an entire FI system structure viewpoint, the reliability model is the combined reliability of all the shelters making up the system. As in the individual shelter models, however, most system structures allow the loss of a single shelter without resulting in a system failure. If this is the case, and the bus is designed to allow continued operations with the loss of one or more shelters, the reliability model is as indicated on the facing page.

A hypothetical system was analyzed which consists of eight shelters and ten devices per shelter. Allowing for the loss of a single device per shelter or the loss of one of the eight shelters, the system MTBF is about 4×10^7 hours. A maintenance concept of "repair immediately upon failure" and an MTTR of 0.25 hour was assumed for the calculations. If the model is changed to exclude the loss of a single device and only account for the loss of a single shelter, the estimated MTBF reduces to about 1.5×10^6 hours. As in the case of a single shelter, system reliability could also be improved through the use of design features such as redundant bus cables or bus interfaces.

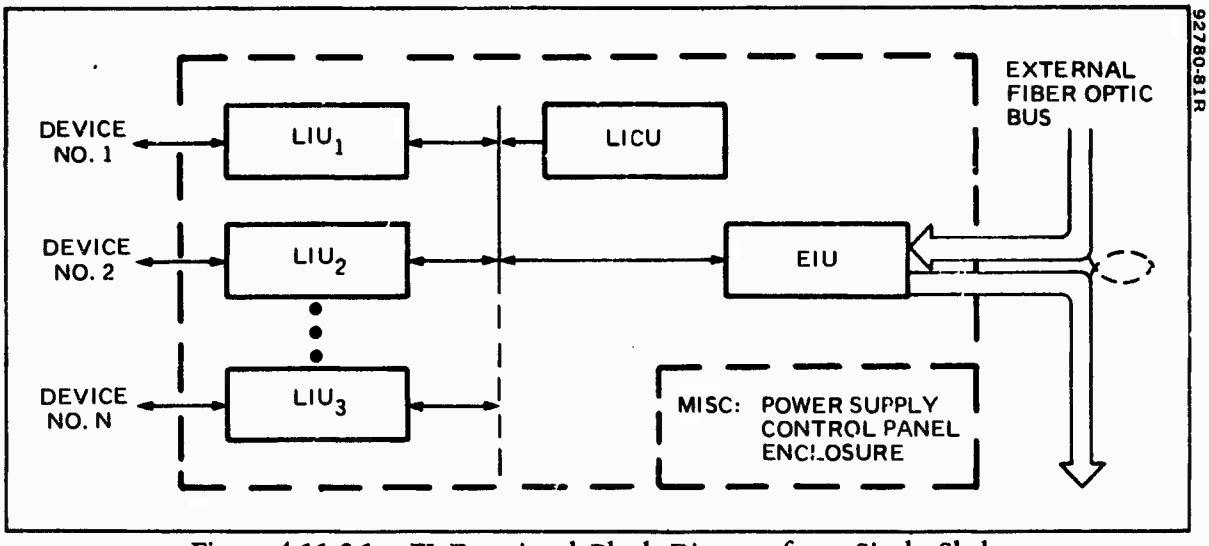
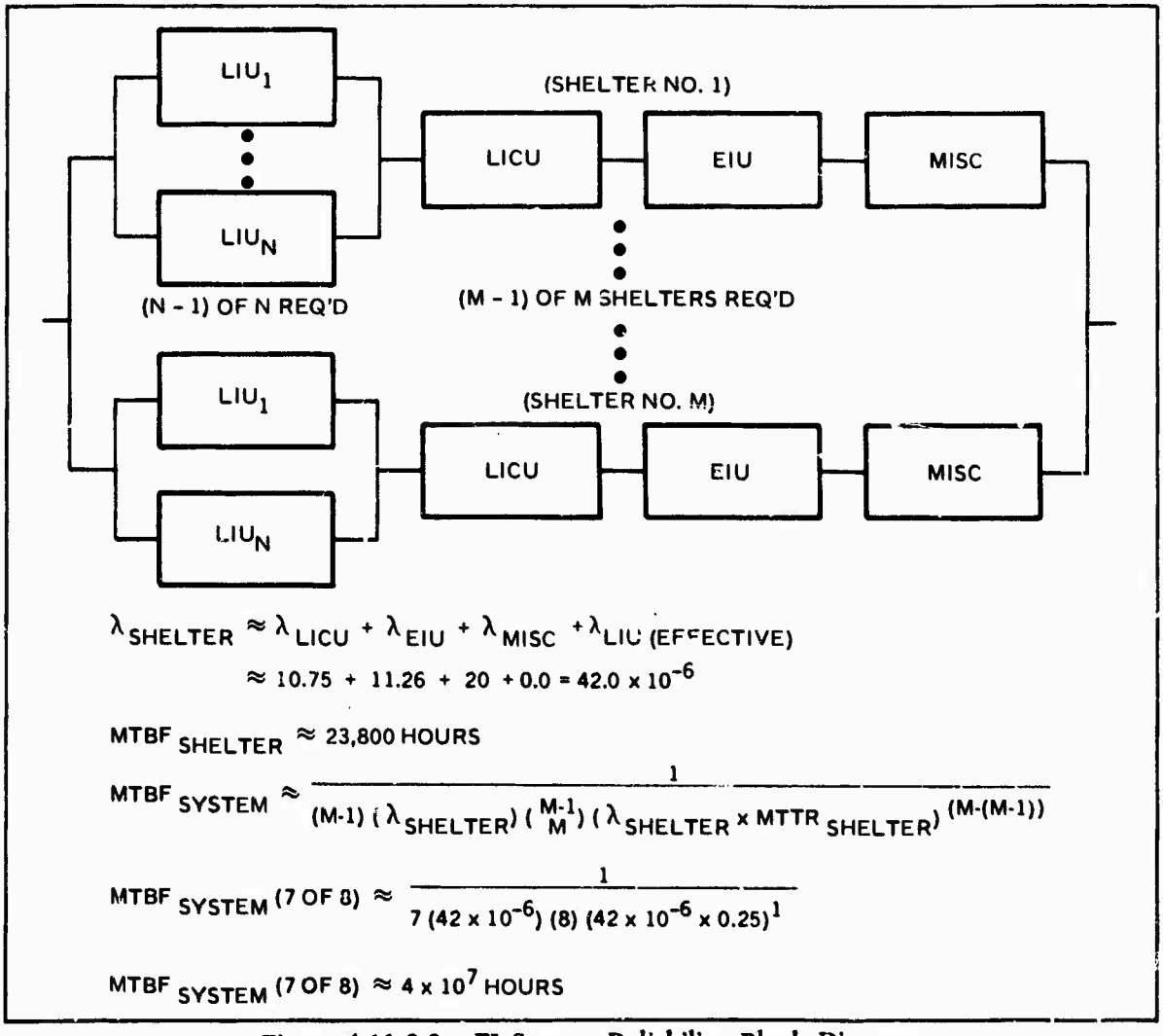


Figure 4.11.2-1. FI Functional Block Diagram for a Single Shelter



$$\lambda_{SHELTER} \approx \lambda_{LICU} + \lambda_{EIU} + \lambda_{MISC} + \lambda_{LIU\ (EFFECTIVE)}$$

$$\approx 10.75 + 11.26 + 20 + 0.0 = 42.0 \times 10^{-6}$$

$$MTBF_{SHELTER} \approx 23{,}800 \text{ HOURS}$$

$$MTBF_{SYSTEM} \approx \frac{1}{(M\text{-}1)\,(\lambda_{SHELTER})\,\binom{M-1}{M}\,(\lambda_{SHELTER} \times MTTR_{SHELTER})^{(M-(M-1))}}$$

$$MTBF_{SYSTEM\ (7\ OF\ 8)} \approx \frac{1}{7\,(42 \times 10^{-6})\,(8)\,(42 \times 10^{-6} \times 0.25)^{1}}$$

$$MTBF_{SYSTEM\ (7\ OF\ 8)} \approx 4 \times 10^{7} \text{ HOURS}$$

Figure 4.11.2-2. FI System Reliability Block Diagram

SECTION 12
FI CAPACITY AND RESPONSE TIME ANALYSIS

Part 4 – Task III, Preliminary Design Analysis
Section 12 – FI Capacity and Response Time Analysis

1. APPROACH TO ANALYSIS

A set of 12 Government - specified load configurations was used to evaluate the FI design in terms of throughput and response time (delay).

An analysis was conducted to evaluate the performance of the FI design under a number of load conditions. The loads and corresponding FI configurations were specified by RADC along with ground rules for their application to the FI design. The table lists eleven load/configurations. A twelfth configuration (Case ℓ) was defined separately as follows:

Case ℓ, Other Traffic Loading: Other traffic is assumed to exist at a rate equal to one-tenth of the Local Intraconnect basic transmission rate (defined below). This traffic is randomly distributed among eight LIs while assuming a probability of 0.7 that the traffic will remain within the originating LI. There are ten LIUs per LI generating this random traffic.

Traffic for Cases a., b., c., d. and e. are treated as separate conditions; traffic for cases f through ℓ is cumulative. That is, Case f, includes traffic for Case e., Case h. includes traffic for Cases e., f., and g., etc. The number given for LIUs per LI is based on the total number of LIUs involved for each case. The ground rules for the analysis, as defined by RADC were;

- A one-hundred percent off-hook factor is assumed for all telephones. Telephones are assumed to be operating at 64,000 bits per second. The discs are operating at a rate of 25 milliseconds per block; the processors are working with the discs at the same rate. All blocks are full 1024, 18-bit words.
- Local Intraconnect operation and External Intraconnect operation are completely asynchronous.
- The effects of crypto interfaces are not to be considered.
- Block transmission is under complete positive control (except for Broadcast) in that a block is not forwarded to a receiver until the receiver has buffer memory space available for storage of the block.

The load conditions were applied to six combinations of possible LI and EI capacities. The specified capacities are in terms of Mb/S for the LI and EI, respectively.

(1) 50, 100 (2) 100, 50 (3) 100, 000
(4) 100, 200 (5) 200, 100 (6) 200, 200

(These capacities are not identical to the FI design (LI = 90 Mb/S, EI = 60 Mb/S) described in this report. They were selected to provide a common framework for comparison of the two contractors' designs.)

The FI performance parameters investigated in the analysis were:

- Throughput - determination of blocks per second and bits per second transferred over the FI under each load configuration. Throughput is the total number of messages (bits) sent to all receivers in one second. A throughput many times greater than the bus bit rate can be achieved if messages are broadcast, or sent simultaneously to more than one receiver.

- Response Time (Delay) - determination of message delay through the FI.
- Probability of Block Delay - time of transit of a block from entry at the source PSI to the receiver PSI.
- Probability of Blockage - the probability that a given load configuration will result in FI blockage, halting all transmissions.

TABLE 4.12.1-1. LOAD CONDITIONS

a.	1 Local Intraconnect	5 telephones	(1 LIU)
b.	1 Local Intraconnect	50 telephones	(5 LIUs)
c.	3 Local Intraconnects	5 telephones each	(1 LIU per LI)
d.	3 Local Intraconnects	50 telephones each	(5 LIUs per LI)
e.	8 Local Intraconnects	100 telephones each	(10 LIUs per LI)
f.	8 Local Intraconnects	2 discs and 2 processors each	(14 LIUs per LI)
g.	8 Local Intraconnects	1 11 megabit per second channel to seven other LI's	(15 LIUs per LI)
h.	8 Local Intraconnects	One virtual bus at one megabit per second with two members per LI	(17 LIUs per LI)
i.	8 Local Intraconnects	One virtual bus at five megabits per second with two members per LI	(19 LIUs per LI)
j.	8 Local Intraconnects	One virtual bus at ten megabits per second with two members per LI	(21 LIUs per LI)
k.	8 Local Intraconnects	Two Lazy Susan buses operating at two megabits per second. Each Lazy Susan bus has four members; each member is on a different LI.	(22 LIUs per LI)

2. THROUGHPUT ANALYSIS

Throughput of the 1, 3 and 8 shelter configurations for various loads were computed. The load having the highest throughput (case ℓ) of 437 megabits per second far from saturates the FI.

In general, the throughput of a network is related to network capacity, the timing structure, transfer protocol and the error rate of the network. Low throughput may result from inefficient timing design, loss of messages due to collisions or the need to retransmit messages in the event of errors.

The Hughes FI design provides a high throughput because:

- a reservation method for bus access is used, thus eliminating collisions.
- an efficient timing scheme allows for productive use of propagation times.
- handshake techniques are used which ensure positive control of message transfers. Messages are not sent unless the receiver is ready to accept them.

Throughput was calculated using the following guidelines:

- Errorless operation is assumed (per SOW)
- Block and Lazy Susan messages are considered to be point-to-point transmissions
- Virtual Bus messages are broadcast type messages sent to all VB members.

Because of the Hughes FI design approach and the manner in which the loads were specified, the bus throughput is the sum of the specified device data rates with the exception of the VB as noted above.

The throughput for the twelve load cases defined in Section 4.12.1 are given in the table in terms of blocks per second and megabits per second for both the LI alone and for the entire FI. Also indicated are the throughputs for each mode of bus transfer: Block, Virtual Bus, and Lazy Susan.

The FI configuration used in the analysis consists of one or more LIs (Shelters) tied into the external intraconnect (EI) portion of the FI. The second column of the table indicates the number of LIs used in each case as defined by the SOW. For cases a thru g data does not leave the LI to which the data source was connected. In cases h thru ℓ, a portion of the data traverses the EI and flows into LIs other than the source LI.

In Virtual Bus modes, the source data is transmitted to all members of each Virtual Bus. Therefore, the total throughput is equal to the source data rate times the number of bus members less 1. (Throughput equals source data rate X (N-1) where N = number of bus members.)

Lazy Susan operation is point-to-point and therefore the throughput is equal to the source data rate on each Lazy Susan bus. In cases k and ℓ there are two Lazy Susan buses operating at 2 megabits each.

It should be noted that the loads specified in the 12 cases far from saturate the FI. Bus efficiency at maximum loads is discussed in Section 4.12.10.

TABLE 4.12.2-1. FI THROUGHPUT

Case	# of LIs	Throughput per LI					FI Throughput				
		Block Messages B/s*	Block Messages Mb/s **	VB Mess. Mb/s	LS Mess. Mb/s	Total Mb/s	Block Messages Mb/s*	Block Messages Mb/S*	VB Mess. Mb/s	LS Mb/s	Total Mb/S
a	1	174	3.2	0	0	3.2	174	3.2	0	0	3.2
b	1	174	3.2	0	0	3.2	174	3.2	0	0	3.2
c	3	174	3.2	0	0	3.2	522	9.6	0	0	9.6
d	3	174	3.2	0	0	3.2	522	9.6	0	0	9.6
e	8	347	6.4	0	0	6.4	2778	51.2	0	0	51.2
f	8	507	9.35	0	0	9.35	4058	74.8	0	0	74.8
g	8	1104	20.35	0	0	20.35	8832	162.8	0	0	162.8
h	8	1104	20.35	1	0	21.35	8832	162.8	15	0	177.8
i	8	1104	20.35	6	0	26.35	8832	162.8	90	0	252.8
j	8	1104	20.35	16	0	36.35	8832	162.8	240	0	402.8
k	8	1104	20.35	16	4	40.35	8832	162.8	240	4	406.8
ℓ	8	1312	24.18	16	4	44.18	10496	193.4	240	4	437.4

* Blocks per second * Megabits per second

3. RESPONSE TIME (DELAY) ANALYSIS

The FI response time analysis was performed by using a simulation program to analyze the LI and a math model to determine delays in the EI.

The delays in the FI include hardware delays (due to memory access time and logic), propagation delays, message transmit time, transmission control delays and bus access delays. All but the last are fixed delays which depend upon intraconnect implementation and the deployment configuration. Message transmit time is fixed for the purpose of this analysis since, by definition, all messages are one Block (1024 words) long. Buss access delay is a function of the relative time of arrival of transmit requests from users. Since transfer requests are random in nature depending on device type and instantaneous data rates, the bus access delay must be considered as a statistical problem.

The FI consists of a Local Intraconnect (LI) and an External Intraconnect (EI) each having its own characteristics. The delay analysis can therefore be performed in two steps. Due to the statistical nature of bus access requests and because of various types of devices and data rates, a simulation approach was deemed best to examine Block message delays in the LI. A math model was adequate for EI delay calculations.

The specific message path for the delay analysis is defined by the load description in the SOW (see case a through ℓ). However, in all cases, the delay path is considered to be from the LI side* of the transmitting LIU to the PSI side of the receiving LIU. For Cases a and b only a single LI and associated LIUs are in the delay path. For Cases c – g several LIs and their associated LIUs are in the path, and an EI is added to the delay path in Cases h – ℓ).

The simulation program is used to compute the bus access waiting time. This is defined as the time interval between a "message ready" signal generated by the LIU and the polling of that LIU by the LICU. The other delays in the transfer path (hardware, transmit, control, etc) are manually added to determine the overall LI delay.

In the FI design, time allocated to Virtual Bus and Lazy Susan transmissions is obtained by interrupting the transfer of Block messages. Therefore, in those cases (h – ℓ) which employ a VB or LS, the delay must be increased by an amount of time equal to the VB and LS interruption time. This time is a variable and is determined by the message capacity allocated to the VB and LS. In the simulation, appropriate VB and LS times are added to the Block transfer delay each VB/LS cycle time of 100 μs. (Cycle time depends on VB/LS message loads; 100 μsec is adequate for the loads specified for this analysis.)

Since bus access time depends to some extent on device starting time, a mean starting time is computed for each device. (See Section 4.12.4 for further discussion).

*The delays in the sending LIU were not considered since it was assumed that a message is always ready at the LIU for transfer to the LI bus.

The EI model is based on the following assumptions:

- the average data rate from each of the eight shelters is equal.
- Block messages are always 1024 words of 18 bits long.
- receiver memories are always available.

In accordance with the SOW and guidance provided by Government Personnel, the error rate was assumed to be zero and therefore delays due to retransmission of erroneous messages are not a factor in the analysis.

The table summarizes the assumptions used in the delay analysis.

TABLE 4.12.3-1. ANALYSIS ASSUMPTIONS

LI Analysis	EI Analysis
Transmit time equals time to transmit one full message (1024 words)	Transmit time equals time to transmit one full message (1024 words).
Number of users depends on case configuration.	The total number of users (LIs) is 8.
Each device transmits one message only for each access to the bus.	Each LI transmits one message during its transmitting cycle.
The receiving DTE memory is always available. Therefore receiver status is not considered.	The receiver is always ready to receive.
Only Case ℓ has outbound messages. The data transferred to the EI (3% of the LI rate) is assumed to be equally distributed over the 8 LIs.	Outbound Block message data rates are equally distributed to the 8 LIs.
The time required for setting up message transfers from LIU to DTE is not considered since it is short compared to the transmit delay.	
The LI access waiting time is a function of device starting time. An average of many starting times of the devices is used in the simulation.	
Delays due to VB and LS interruptions are added to the Block message delay.	
Delay of LIU access to the LI due to higher priority of an EIU is not considered since the incoming message rate is very low.	
Virtual Bus and LS message delay is not computed. TheVB and LS use of a fixed timing structure and therefore the delay is fixed.	

4. DESCRIPTION OF THE LI SIMULATION PROGRAM

The use of a simulation program to determine LI bus access delay provides the ability to more accurately account for varying data rates and random device start times.

Based on the assumptions described in Section 4.12.3 a program was written to simulate the LI structure. The simulation is aimed at determining LI bus access delay for Block messages. Fixed delays such as message transmit delay, the time to accomplish PSI "handshake" and other hardware delays are not included in the simulation since these fixed delays can simply be added to the bus access delay to obtain the total delay.

In the Hughes FI design, user access to the LI bus is obtained through a reservation technique managed by the LICU. The LIU associated with the source device generates reservation information regarding its message for transfer to the LICU when the LIU is polled. This information is contained in two words and allows the LICU to check the status of the receiver. Assuming the receiver is available, the LICU sends a transmit enable signal to the LIU and the message is then transferred to the bus.

In the simulation the LICU is represented by a timer which is appropriately incremented by time periods equal to the time it takes to perform each step in a message transfer. The timer is used as a reference from which all other times are measured.

Two factors prescribe the design of the simulation program: (1) the relative start times of all the devices on the FI affects LI bus access delay, and (2) for any given set of device start times, access delays vary for each message transmitted by each LIU. The latter delay depends on the relative data rates of each device on the bus. To account for these variables, two cycles have been designed into the simulation.

New sets of device start times are computed S_D times (an input parameter) and the number (J) of polling cycles run for each starting time (also an input parameter). The average bus delay for each LIU on each polling cycle is then computed. These delays are then averaged over all LIUs for each polling cycle, over the J polling cycles, and over the S_D number of start cycles. In addition, the maximum delay encountered in the simulation is recorded.

The average LI bus access delay (D) then, is the average delay of all messages.

$$D = \frac{W_{(i)}}{\sum_{i=1}^{I} N(i)}$$

where $W_{(i)}$ = the access delay of message from $LIU_{(i)}$.

N(i) is determined by the number of devices in a given case and their data rates.

The simulation program is depicted in the flow chart. The simulation is initiated by selecting one of the 12 cases whose parameters have been preset into the program. Device starting times are selected using a random number generator. The LICU "Timer" is set to zero and the polling sequence begun. When an LIU is polled, and if it has no message to transmit, a time equal to that needed to transfer two LIU message information words is added to the LICU "Timer." If a message is ready, the LICU "Timer" is increased by a time equal to the two words plus the message transmit time (TT), where TT is the time needed to transmit one block. The "Wait Time" (access delay) is then computed. "Wait Time" is the time an LIU has to wait to be polled after a message is ready for transmittal. It is a function of the number of devices and their data rates.

In the FI design, when the polled LIU has no message ready for transmittal, the next LIU in sequence would be polled, and so on until an LIU with a "message ready" has been found.

To facilitate the simulation, this sequence of actions has been replaced with a rountine which determines the time when the next message would be ready based on the specified devices and their data rates. If this time is greater than the time it takes the LICU to poll each LIU (the polling cycle time), the "Timer" is increased by an amount equal to the polling cycle time.

Since VB and LS transmissions are accomplished by interrupting Block message transmissions, the "Timer" must be incremented each 100 microseconds (LI cycle time) by the amount of time required to transmit VB and LS messages.

After "J" polling cycles are completed, a different set of device starting times is selected and the simulation run again. After S_D sets of starting times, the computed delays are averaged. This average value is defined to be the LI bus access time.

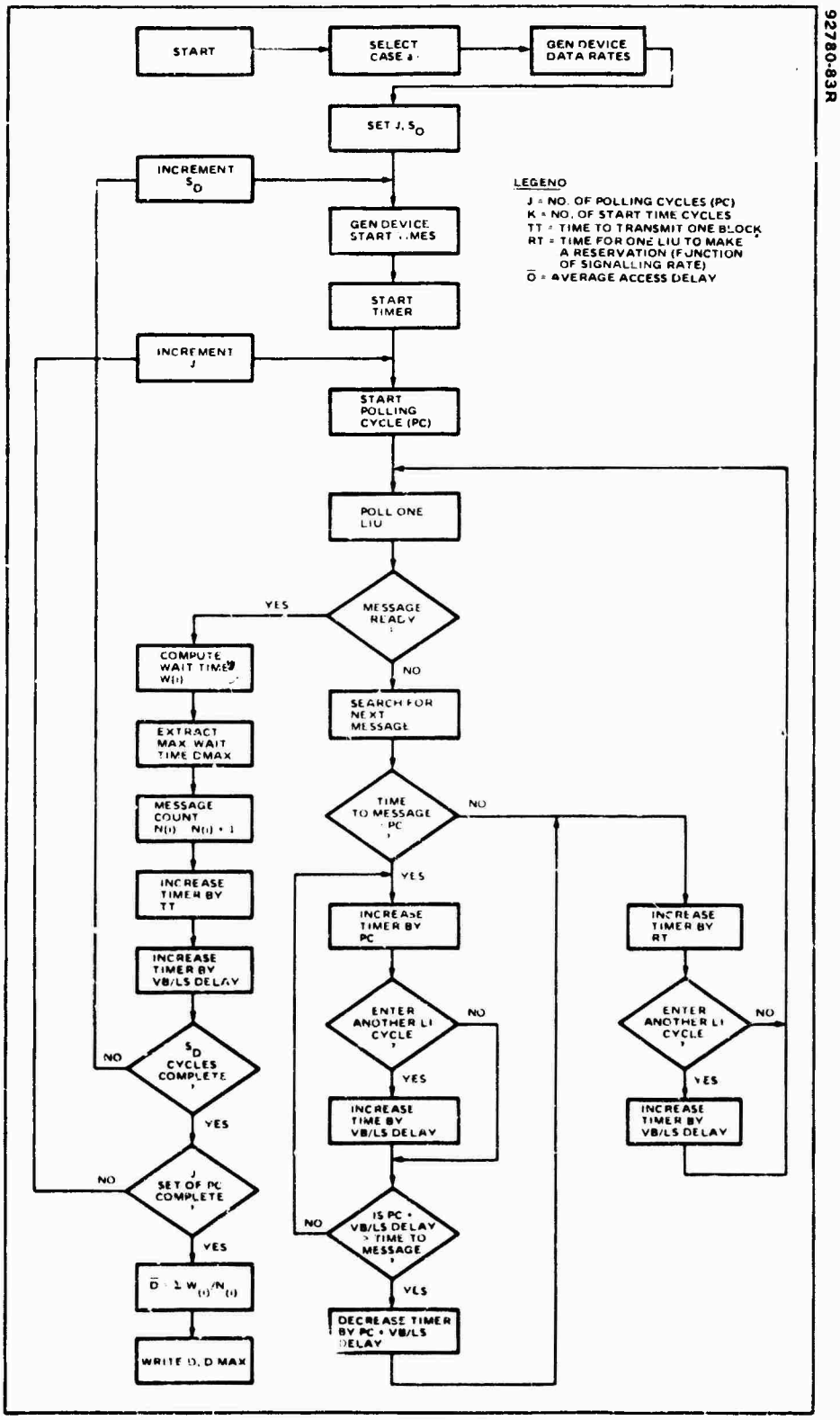


Figure 4.12.4-1. LI Simulation Flow Chart

5. LI RESPONSE TIME (DELAY)

For the heaviest load, the average waiting time for access to the LI bus varies from 55 microseconds to 5.1 microseconds for the 50 Mb/s and 200 Mb/s signalling rates respectively.

The total LI response time is the message transfer delay from the PSI of the source LIU to the PSI of the receiving LIU. This includes the message buffering delay, LI bus access delay, and processing delays. Processing includes error checking and message header formatting and are insignificant in the Hughes design. The PSI transfer "handshake" set up is small and can be omitted in the computation of response time.

The LI bus access delay is a function of the device data rates and bus signaling rate. It reflects the performance of the system architecture including such factors as timing design and transfer protocols. The bus access delay is a major contribution to the total transfer delay, especially in high data rate systems.

Message transmit delay is a function of message length and the bus signaling rate. For 1024 18-bit word messages this is another large contributor to the total delay. Transmit delay and processing delays are fixed delays while bus access delay varies from message to message.

The average access delay computed by means of the simulation described in the previous topic is used in calculating the total LI delay. Processing delay in the LIU is estimated to be 40 μs. The message transmit delays for the three signaling rates are as follows:

368 μs 50 Mb/s signaling rate
184 μs at 100 Mb/s signaling rate
92 μs at 200 Mb/s signaling rate

The total LI delay is the sum of the processing delay, the message transmit delay and the bus access delay. The results are indicated in the table.

The maximum delay encountered in each case (totaling about 700 messages) is indicated.

Cases a and c have no entries since in the Hughes design the five telephones are connected to one LIU. No information is transferred via the LI and therefore there are no delays.

TABLE 4.12.5-1. MESSAGE TRANSFER DELAY IN THE LI

	50 Mb/s BUS						100 Mb/s BUS					200 Mb/s BUS				
Case	Data Rate	LI Access Delay Ave.	LI Access Delay Max.	Buff & Processing Delay	Total Ave.	Total Max.	LI Access Delay Ave.	LI Access Delay Max.	Buff & Processing Delay	Total Ave.	Total Max.	LI Access Delay Ave.	LI Access Delay Max.	Buff & Processing Delay	Total Ave.	Total Max.
a	–	–	–	550	–	–	–	–	366	–	–	–	–	274	–	–
b	3.2	5.3	219		555	769	3.5	179		369	545	0.54	64		275	338
c	–	–	–		–	–	–	–		–	–	–	–		–	–
d	3.2	5.3	219		555	769	3.5	179		369	545	0.54	64		275	338
e	6.4	10	368		560	918	3.8	165		370	531	2.2	94		276	368
f	9.35	17	439		565	989	5	165		371	531	1.4	39		275	313
g	20.35	16	723		566	1273	4.9	182		371	548	2.5	130		277	404
h	21.35	16	735	557	573	1292	5	185	368	373	555	2.5	131	275	278	405
i	26.35	20	791	594	614	1385	5.4	195	377	382	572	2.7	133	277	280	410
j	36.35	31	994	668	699	1662	7.3	231	395	402	627	3.1	148	281	284	429
k	40.35	38	1066	697	735	1763	8.1	243	403	411	646	3.5	155	283	287	438
ℓ	44.39	55	1011		752	1708	12	414		415	817	5.1	100		288	388

Data Rate in megabits per second (MB/s)
Delay in microseconds
Buff & Processing Delay – Buffering and processing delays at source and destination LIUs.

6. EI RESPONSE TIME (DELAY) ANALYSIS

A mathematical model was developed to analyze EI response time.

EI response time was analyzed using the eight shelter configuration defined in the statement of work. The eight shelters are identical and it was assumed that the data transfer rates to the EI from all shelters were equal. Using these assumptions, a mathematical model was developed for analysis of EI response (delay time).

The analysis was made using the timing structure developed during the Task I, II, and III Study Phases. The timing structure consists of cycles each divided into Message Count, Short Message, Transfer Request, Transfer Grant, Block Message, VB and LS and ACK/NACK segments as depicted in Figure 4.12.6-1. The Message Count contains 8 slots, each assigned to one user (shelter). The Block transfer segment is configured to be capable of transmitting one maximum block message, or 1024 18-bit words. The VB and LS portions are configured to satisfy the capacity defined in the SOW. The duration of the cycle time depends on the bus signalling rate (50, 100, or 200 Mb/s); the higher the signalling rate, the shorter the cycle time.

Since bus access waiting time (delay) depends on the traffic load, a statistical average of delay times is used to evaluate the performance of the EI. Assuming the probability of message generation from user i is P(i), there exists a probability for each of either situations, i.e., the probabilities of no message transmission, one message transmission, etc., up to eight consecutive message transmissions. (P(i), then, = R(i)/C, where R(i) is the device data rate and C is the bus capacity. To simplify the analysis, it is assumed each user transmits one message at a time. The probability of no message transfer is the probability that none of the eight users has a message ready when the cycle starts. The probability of one message transfer is the probability that any one of the eight users has a message ready for transfer, and so forth. The probability of eight consecutive message transmissions can be found in the same way. The probabilities of these cases are:

$$P(0) = \binom{8}{0}(1-P)^8 \text{ for no message transmission}$$

$$P(1) = \binom{8}{1}P(1-P)^7 \text{ for one message transmission}$$

$$P(2) = \binom{8}{2}P^2(1P)^6 \text{ for two consecutive message transmissions}$$

$$\vdots \qquad \vdots$$

$$P(8) = \binom{8}{8}P^8 \text{ for eight consecutive message transmissions}$$

For each message transmission, a cycle time (T_c) is used. Therefore the average waiting time is:

$$\bar{D} = \sum_{i=0}^{8} P(i)\, iT_c$$

As depicted in Fig. 4.6.12-2 the initial delay inherent in the timing structure must be added to the average waiting time to obtain the bus access delay. Using cycle N as a reference, if a message is ready at the beginning of the Nth cycle, the initial delay is minimum, (denoted as Tmin.). If the message is ready just after the beginning of the N-1th cycle, the initial delay is maximum, (denoted as Tmax.). To simplify the problem, an average is used for the initial delay. The average bus access delay is then found as:

$$W = \frac{Tmin + Tmax.}{2} + \sum_{i=0}^{8} P(i)\, iT_c$$

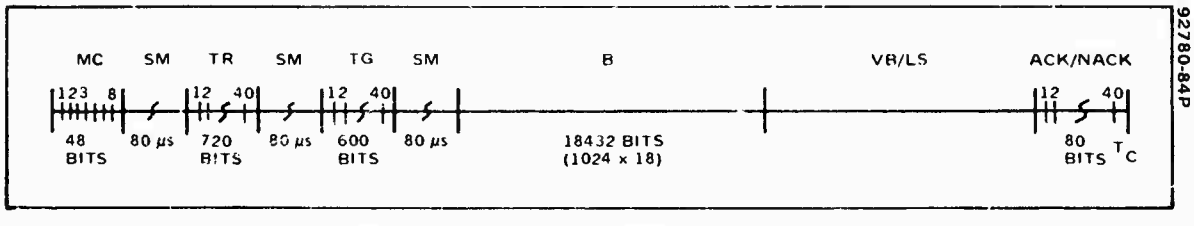


Figure 4.12.6-1. EI Timing Structure

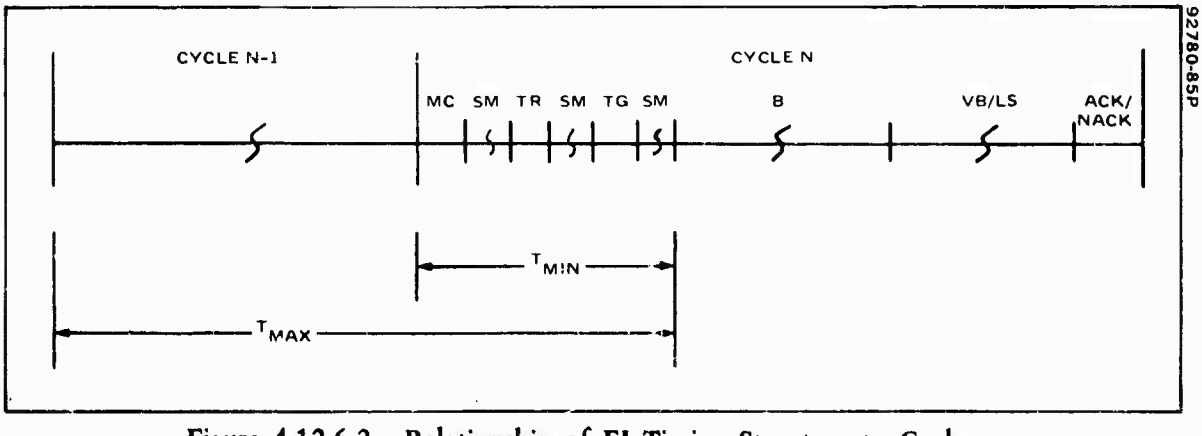


Figure 4.12.6-2. Relationship of EI Timing Structure to Cycles

7. EI RESPONSE TIME (DELAY)

The factors affecting EI response time are the message buffering time, bus access waiting time, hardware processing delay and propagation delay.

Message buffering delays occur at both the source and the destination EIUs. (The center segment of Fig. 4.12.8-1 illustrates the following discussion.) The time required to store a message in a buffer depends on the bus transmission rate and is equal to the time required to transmit a block. The source EIU buffer rate is a function of the LI bus signaling rate while at the destination EIU, the buffering rate is a function of the EI bus signaling rate. The message transmit time at various signaling rates are 368 μs at 50 Mb/s bus signaling rate, 184 μs at 100 Mb/s and 92 μs at 200 Mb/s. (Storing a complete message in the EIU before further transmission serves two purposes. At the source EIU, the delay is necessary for bit encryption and simple transmission control. At the destination EIU buffering of a complete message facilitates bit decryption.)

The bus access waiting time is computed using the model described in Section 4.12.6. The delay depends entirely on the bus signaling rate. The higher the signaling rate, the shorter the access waiting time. This is because the cycle time is reduced at higher signaling rates, thus shortening both the initial delay and the delay caused by non-availability of the bus due to other message transmissions. Using the three specified bus capacities, (50 Mb/s, 100 Mb/s and 200 Mb/s,) P(i), the cycle time T_c, Tmin. and Tmax. are computed to obtain the average delay D as indicated in the tables.

The duration of T_c, Tmax and Tmin depends on the bus signaling rate. These durations, in microseconds are:

	50 Mb/s	100 Mb/s	200 Mb/s
T_c	1062	548	377
T_{max}	1329	802	624
T_{min}	267	254	247

The above description reflects the FI design developed by Hughes during the study phases. In this design a direct interface was implemented between the LI bus and the EIU. An alternative way of implementing the EI-LI interface is to use an additional LIU. Additional buffering delays are then introduced due to the additional LIU buffering at both the source and the destination. The buffering delay in the source LIU* is the time required to transmit a message at the LI signaling rate (50, 100, 200 Mb/s). The delay due to the additional LIU*, based on the 180 Mb/s standard interface transfer rate between EIU and LIU*, 102.4 μsec per block. The destination EIU buffering delay is the time required to transmit a block message at the EI bus signaling rate (50, 100, 200 Mb/s).

The hardware processing delay includes transfer processing between LIU and EIU and between the EIU and EI, all at the source; and the delays of transfer handshake from EIU to LIU and the transfer between the LIU and the LI at the destination. These processing delays are estimated to be about 40 microseconds.

Note: LIU* - This symbol has been used to distinguish between LIUs which in the basic design interface the LI with each device, and the LIU (whose design is identical) that interfaces the LI with the EIU in the alternate design.

Propagation delay is approximately 80 microseconds with the source - destination distance of 16 Km used in the analysis.

The EI delays were computed for two designs: (1) a direct connection between the EI and the LI as in the Hughes basic design, and (2) the EIU-LI interface via an LIU. Tables 4.12.7-1 and -2 indicate the values of the celay elements for design (1) and (2) respectively. Table 4.12.7-3 summarizes the delays for both designs.

The additional delay due to the added LIU* (design 2) is 245 microseconds an increase of 13% for an EI bus with the lowest signalling rate and an increase of 30% for an EI bus having the highest signalling rate.

TABLE 4.12.7-1. ELEMENTS OF EI DELAY** – EIU DIRECTLY CONNECTED TO LI

	EI Signalling Rate								
	50 Mb/s			100 Mb/s			200 Mb/s		
LI Signalling Rate (Mb/s)	50	100	200	50	100	200	50	100	200
LI/EIU Buffer & Processing Delay	-	241	-	535	241	121	-	241	121
EIU/EI Access Delay (Average)	1003 μs			582 μs			489 μs		
Propagation Delay	80 μs			80 μs			80 μs		
EI/EIU Buffer & Processing Delay	388 μs			204 μs			112 μs		
EIU/LI Access Delay	0			0			0		
Total EI Delay	-	1711	-	1401	1106	987	-	922	802

** All delays are in microseconds

TABLE 4.12.7-2. ELEMENTS OF EI DELAY** – EIU CONNECTED TO LI VIA AN LIU

	EI Signalling Rate								
	50 Mb/s			100 Mb/s			200 Mb/s		
LI Signalling Rate (Mb/s)	50	100	200	50	100	200	50	100	200
LI/LIU* Buffer & Processing Delay	-	241	-	535	246	126	-	246	121
LIU*/EIU Buffer & Processing Delay	122.4 μs			122.4 μs			122.4 μs		
EIU/EI Access Delay (Average)	1003 μs			582 μs			489 μs		
Propagation Delay	80 μs			80 μs			80 μs		
EI/EIU Buffer & Processing Delay	388 μs			204 μs			112 μs		
EI/LIU* Buffer & Processing Delay	122.4 μs			122.4 μs			122.4 μs		
LIU*/LI Access Delay	0			0			0		
Total EI Delay	-	1957	-	1646	1352	1232	-	1167	1047

TABLE 4.12.7-3. EI MESSAGE TRANSFER DELAY**

	EI Signalling Rate					
	50 Mb/s		100 Mb/s		200 Mb/s	
LI Signalling Rate	EIU Direct	EIU via LIU	EIU Direct	EIU via LIU	EIU Direct	EIU via LIU
50 Mb/s	2006	2251	1401	1646	1216	1461
100 Mb/s	1711	1957	1106	1352	922	1167
200 Mb/s	1592	1837	987	1232	802	1047

** All delays are in microseconds.

8. FI RESPONSE TIME (DELAY)

Total FI delay is the sum of the delays of the source LI, the EI and the destination LI. Delays for FIs using six combinations of signalling rates were determined.

The FI response time (total message delay) is defined as the sum of the delays from the PSI side of the source LIU to the PSI side of the destination LIU. The delay model, shown in Figure 4.12.8-1, is segmented into three portions: the source LI, the EI and the destination LI. Two implementation schemes are indicated for the EI: (1) (upper path) the basic Hughes design, an (2) a design which includes an LIU between the EIU and the LI.

The EI delay at the source shelter consists of the LI/EIU buffer time and EIU to EI access time for design (1) It consists of the LI to LIU buffer time, the LIU to EIU buffer time, and the EIU to EI access time for design (2) at the destination shelter, the EI delay consists of the EI to EIU buffer time for both designs. For design (1) an additional delay for EIU to LI access time exists, while for design (2) additional EI delays consist of the EIU to LIU buffering time plus the LIU to LI access time. The destination LI delay for both designs is the LI to LIU buffer and processing times.

The bus access delay and the message buffering delay in the LIU at the source end of the EI are a function of the LI signalling rate. The message buffer delay at the destination EIU is a function of EI bus signalling rate and the buffer delay at the receiving LIU is a function of the destination LI bus signalling rate. The LIU to EIU interface at the source and the EIU to LIU interface at the destination are 180 Mb/s interfaces thus requiring 102 microseconds to transfer one block of 1024 words. Transmission times are 368 microseconds for a 50 Mb/s bus, and 184 and 92 microseconds for 100 Mb/s and 200 Mb/s busses.

The EIU/LI and LIU*/LI access delays were assumed to be zero since these units have the highest priority for access to the LI. Actually, a delay of a few microseconds may be experienced.

Other delays include the processing delays, the bus access delay, the hardware delays at various parts of the model and propagation delays. The processing delay at the source and the receiving LIUs include header processing and PSI message transfer set up and is estimated to be 40 microseconds.

While the message transfer propagation delay is almost zero in the local intraconnect since the bus length is only inches, the propagation delay in the EI bus is significant. At a two mile communication distance the delay is 32 microseconds and for five miles this time is 84 microseconds. In the analysis, the maximum delay (84 microseconds) was used.

Tables 4.12.8-1 and 4.12.8-2 indicate the delays in the three segments of the model and the total delay for the six specified signalling rate combinations. Table 4.12.8-1 reflects the delay in the basic Hughes FI design in which the EIU is directly connected to the LI. Table 4.12.8-2 provides the same data for a design in which the EI is connected to the LI via an LIU. The increase in delay for the latter design is due to the delays of buffering and processing in each of the two additional LIUs* in the message path (one at the source LI and one at the destination LI). The increase in time is about 245 microseconds representing an 11% impact on FI delay for the lowest signalling rate system, and a 22% impact on the highest signalling rate system.

TABLE 4.12.8-1. FI DELAY – EIU DIRECTLY CONNECTED TO LI

Signalling Rate (Mb/s)		Delays (μsec)			
LI	EI	Source LI	EI	Destination LI	Total
50	100	197.4	1401	555.2	2154
100	50	154.4	1711	260.8	2126
100	100	154.4	1106	260.8	1521
100	200	154.4	922	260.8	1337
200	100	146	987	141.2	1274
200	200	146	802	141.2	1089

TABLE 4.12.8-2. FI DELAY – EI CONNECTED TO LI VIA AN LIU

Signalling Rate (Mb/s)		Delay (μsec)			
LI	EI	Source LI	EI	Destination LI	Total
50	100	197.4	1646	555	2398
100	50	154.4	1457	260.8	2372
100	100	154.4	1352	260.8	1767
100	200	154.4	1167	260.8	1582
200	100	146	1232	141.2	1519
200	200	146	1047	141.2	1334

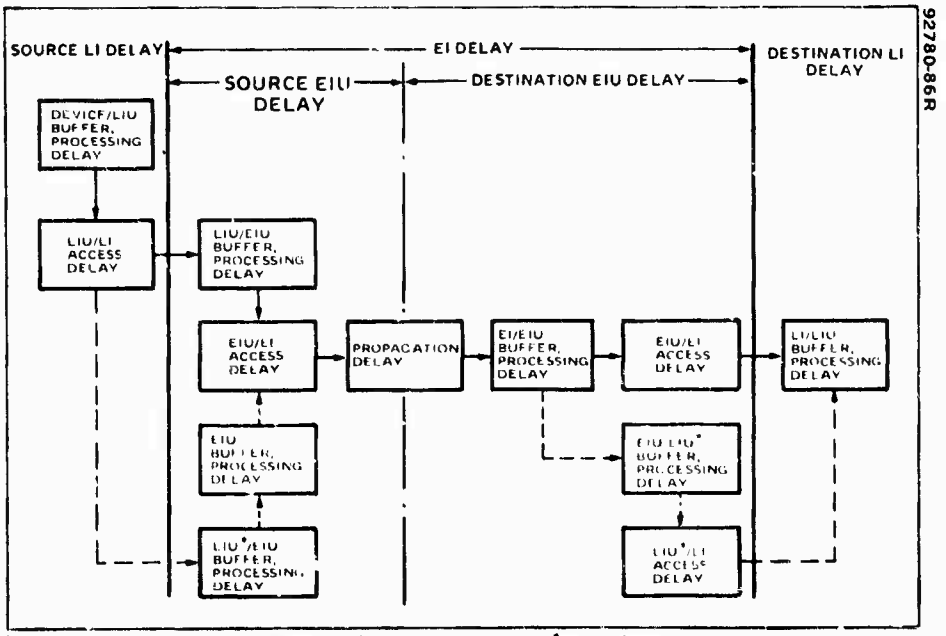


Figure 4.12.8-1. FI Delay Diagram

9. MESSAGE BLOCK DELAY AND FI BLOCKAGE

The Hughes-design of the FI, through its use of positive message flow control, results in very low probabilities of block delay and zero probability of FI blockage.

Block Delay – Message block delay in the Hughes design is essentially a function of EI access delay; LI delays are small in comparison. Therefore, the probability of block delay can be determined by examining the delays in the EI.

The probabilities of block delay are as follows:

$P(0) = \binom{8}{0} (1-P)^8$, the probability of no waiting

$P(1) = \binom{8}{1} P(1-P)^7$, the probability of waiting for one time cycle

$P(2) = \binom{8}{2} P(1-P)^6$, the probability of waiting for two time cycles

. .
. .
. .

$P(8) = \binom{8}{8} P^8$, the probability of waiting for eight time cycles.

The probability of block delay is 1-P(0), or 0.17 for a 50 Mb/s signaling rate, 0.088 for a 100 Mb/s signaling rate and 0.045 for a 200 Mb/s signalling rate.

The probability of block delay versus amount of delay in time cycles (T_c)* is depicted in the curve in Figure 4.12.9-1 for the three bus capacities. As shown in the curves, the probability of a wait for EI access is extremely low. The three figures at the top, left of the curves indicate the probability that a message will be transferred within one time cycle after it is assembled in the source LIU. Most of the messages are transferred within one cycle following the cycle in which the message became available.

It should be noted that Probability of Block Delay is not a continuous function; it exists at discrete cycle times only. The continuous curves were drawn to better indicate the trend of the function.

FI Blockage – Since the FI design employs positive message flow controls and the "front-end handshake" technique ensures that a transfer path is clear, a message is transmitted only when the destination is able to receive it. Therefore, if the data rate is below the maximum bus capacity (98% of the bus signaling rate), the probability of blockage is zero.

*See Section 4.12/7 for values for T_c.

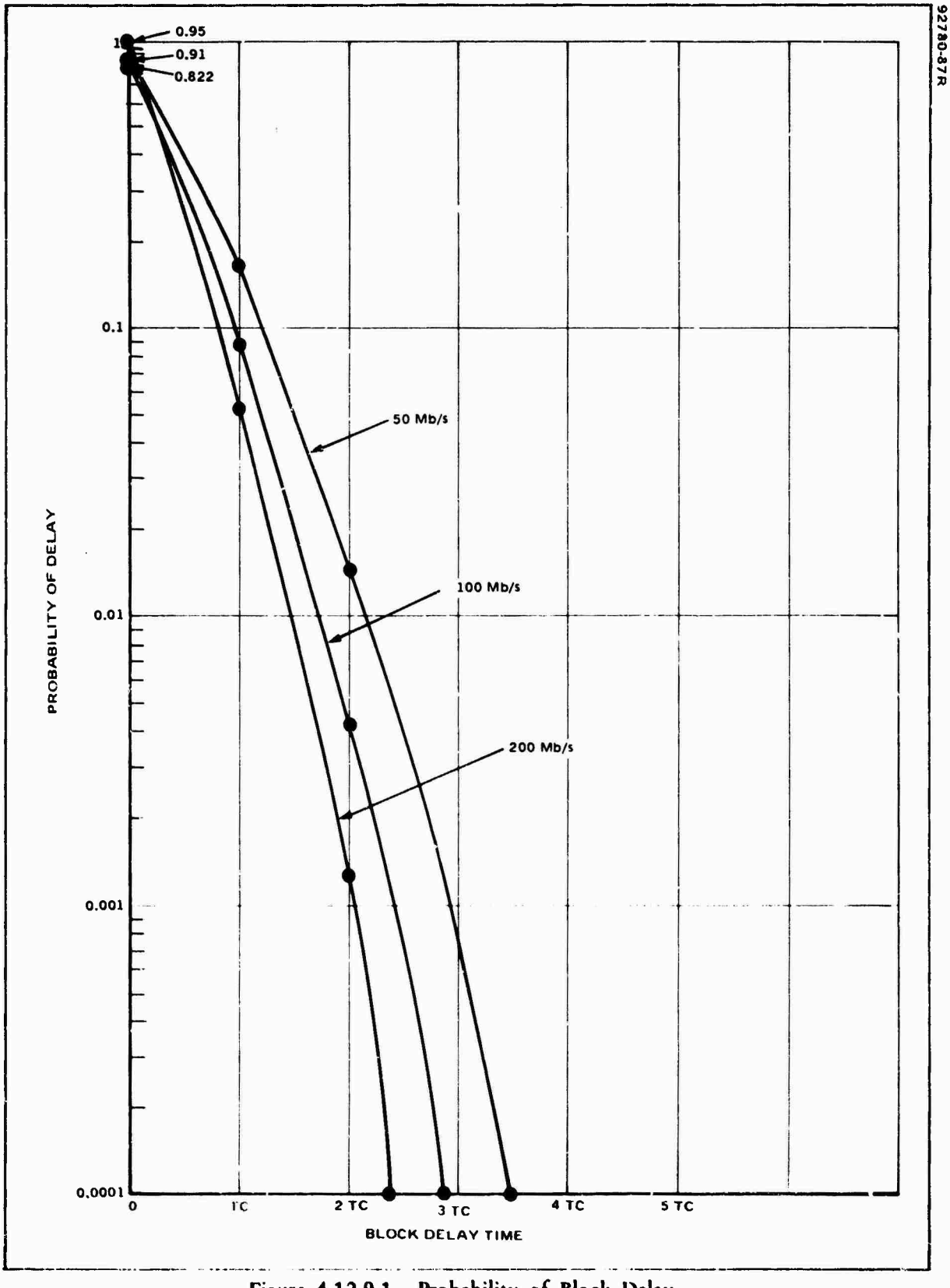


Figure 4.12.9-1. Probability of Block Delay

10. BUS EFFICIENCY AT MAXIMUM LOADS

The load configurations specified in the SOW are substantially below the capacity of the Hughes FI design. Therefore, an analysis of FI efficiency under heavier loads was performed. An efficiency of about 98% exists under maximum loads.

The load postulated for this analysis was based on Case ℓ which requires that 20 Mb/S be used for the Virtual Bus and Lazy Susan. The remainder of the FI capacity was allocated to Block message transfers.

As in the previous analysis, the determination of FI efficiency under maximum load conditions was performed in two steps – LI efficiencies and EI efficiency.

In the LI where transfers are controlled by the LICU, each Block message transfer requires an overhead of four words for front-end handshake, the reservation process, polling by the LICU, and the ACK/NACK. In addition, 10 microseconds was allowed for ACK/NACK processing. These overhead items result in Block message transfer efficiencies (based on slots allocated to Block messages as opposed to full bus capacity) of 96.5% for the 50 Mb/s signalling rate, 94% for the 100 Mb/s rate, and 88% for the 200 Mb/s rate. The upper portion of Table 4.12.10-1 lists the corresponding data rates.

The timing structure for message transfers over the EI contains slots for Short Block messages in addition to Block, Virtual Bus, and Lazy Susan messages. Short Block messages make use of propagation delay times (80 microseconds for a 16 Km bus). These slots can also be used for segmented Block message transfers if the operational systems in which the FI is imbedded does not need the full allocation for Short Block messages.

As in the LI computation, 20 Mb/s are reserved for VB and LS messages. The remainder of the slots are then available to Block and Short Block messages in the amounts shown in the middle part of the table. The analysis assumed that one block is transferred each cycle and Short Block message slots are fixed-assigned to each user (8 shelters in case ℓ).

The last row of the table indicates the overall FI efficiency for the combined message types for each of the three signalling rates.

TABLE 4.12.10-1 FI EFFICIENCY UNDER MAXIMUM LOAD

		Bus Signalling Rate (Mb/s)					
		50		100		200	
		Data Transferred		Data Transferred		Data Transferred	
		Mb/s	% Capacity Used	Mb/s	% Capacity Used	Mb/s	% Capacity Used
LI	Block	29	58	75	75	159	80
	VB/LS	20	40	20	20	20	10
EI	Block	17.36	35	33.6	33.69	48.9	24.4
	Short Block	11.3	22.6	43.8	43.8	127	63
	LB/LS	20	40	20	20	20	10
FI	All Message Types	48.66	97.3	97.4	97.4	195.9	98

PART 5
CONCLUSIONS AND RECOMMENDATIONS

Part 5 -- Conclusions and Recommendations

1. CONCLUSIONS OF THE ANALYSES AND RECOMMENDATION FOR DEVELOPMENT

A practical FI design concept which meets Tactical Air Force Modular C^3 goals has been developed. It is recommended that the preliminary FI design be demonstrated and evaluated in a development program which connects typical C^3 devices into an operational configuration.

The FI design described in this development meets the requirements of current and planned TAF C^3 centers through the 1990s. It fulfills the modularity, flexibility, inoperability, and survivability goals of the Mod C^3 concept. The concept and requirements were developed and analyzed based on a detailed C^3 center configuration and operations analyses. The most cost-effective approach was selected from a set of six design concept candidates, and was verified against requirements of existing and planned C^3 centers, such as the CRC and ATACC, and according to the goals of the TAFIIS Master Plan. The FI not only meets the requirements of C^3 centers but will enhance the growth of those centers into the 1990s with phased implementation of modular equipments, software, and facilities.

The Preferred Standard Interface (PSI) developed in the interface analysis provides the capability, in FI equipped centers, to "plug in" modular equipments, taking advantage of the FI's programmable connectivity. The simple, positively controlled, standard interface allows equipments operating asynchronously, and at their own rate, to exchange data over the FI in message packets. The PSI message protocol provides for software modularity and interoperability via a "layered" approach. A preliminary interface standard was developed with the intent that eventually this standard would evolve to become a military standard which will guide the development of future Modular C^3 equipments. The resulting developments will support phased development and implementation of Mod C^3 centers. For example, as new or more capable display devices, computers, or communications equipments are developed, Modular C^3 centers can be upgraded with those devices without requiring major redesign of the centers. In the interim, existing non-standard devices are accommodated in Mod C^3 centers via Selected Adapter Units, which convert other interfaces to the PSI.

The preliminary FI design incorporates high capacity, configuration flexibility, positive control, and stable operation that can be implemented today, but exploits advanced technology. (The External Intraconnect is designed for fiber optic implementation. Control functions take advantage of microprocessor capabilities and surface acoustic wave devices.) Future growth and development is provided for in the functional and physical modularity of the design. FI connectivity and configuration are controlled by software, providing configuration flexibility and operation that is stable, even in the face of casualty losses and peak loads. The FI electronics package, (all the FI hardware

required in each shelter) can be packaged in less than one-third of a standard 19-inch equipment rack. Reliability analyses predict high reliability with current implementation and very significant reliability improvements in future Mod C^3 systems.

The preliminary design of the FI is completed and is ready to be carried forward in a development program.

CONCLUSIONS:

- The developed FI concept meets TAF MOD C^3 goals,
- A MOD C^3 Standard Interface is defined which promotes C^3 interoperability, and
- The preliminary design exploits advanced technology and is ready to be implemented.

RECOMMENDATION

- Develop the Flexible Intraconnect hardware and software to provide a vehicle for demonstrating and evaluating the concept in a realistic TAF C^3 environment.

GLOSSARY

ACK/NACK	– Acknowledge/Negative Acknowledge
AIU	– Analog Interface Unit
ALCC	– Air Lift Control
ASRT	– Air
AWACS	– Airborne Warning and Control System
B	– Block
BIU	– Bus Interface Unit
C^3	– Command, Control and Communications
CBI	– Control Bus Interface
COMM	– Communications – (related to SCC Shelter)
CPU	– Center Processing Unit
CRC	– Control and Reporting Center
CRP	– Control and Reporting Post
$\overline{D}$	– Average Message Delay
DASC	– Direct Air Support Center
DIU	– Device Interface Unit
DISP	– Display (related to SCC shelter)
DOB	– Data On Bus
DP	– Data Processing (related to SCC shelter)
DRA	– DTE Register Available
DRF	– DTE Register Full
DTE	– Device Terminal Equipment
EI	– External Intraconnect
EIU	– External Intraconnect Unit
ESD	– Electronic System Division
FACP	– Forward Air Control Party
FAX	– Facsimile
FDM	– Frequency Diversity Modulation
FEBA	– Forward Edge Battle Area
FI	– Flexible Intraconnect
FIFO	– First In First Out
FOM	– Figure of Merit
ICS	– Intercommunications System
IDR	– Input Data Request
I/O	– Input/Output
J	– Number of Polling Cycles
JTIDS	– Joint Tactical
Kb/s	– Thousand bits per second
KG	– Key Generator
LD	– Line Driver
LI	– Local Intraconnect
LICU	– Local Intraconnect Control Unit
LII	– Local Intraconnect Interface
LIU	– Local Interface Unit
LR	– Line Receiver
LRA	– LIU Register Available
LRF	– LIU Register Full
LS	– Lazy Susan
LSI	– Large Scale Integrated

Mb/S	– Megabits per second
MOE	– Measure of Effectiveness
MS	– Message Segment
MTBF	– Mean Time Between Failure
MTTR	– Mean Time-to-Repair
MUX	– Multiplexer
$N_{(i)}$	– Any one message from $LIU_{(i)}$
NTDS	– Naval Tactical Data System
ODR	– Output Data Request
PC	– Polling Cycles
PROM	– Programmable Read-Only Memory
PSI	– Preferred Standard Interface
RAM	– Random Access Memory
RES/TRAN	– Reservation/Transmit
ROM	– Read-only Memory
RT	– Time Required by an LIU to make a reservation
S_D	– Number of Device Start Times
SAU	– Selected Adapter Unit
SB	– Sub-Bus
SC	– Self Contained (Related to SCC Shelter)
SCC	– System Configuration Concept
SIU	– Standard Interface Unit (later LIU)
SN	– Sequence Number
SSI	– Shelter-Shelter Interface
SSU	– Shelter-Shelter Unit
ST	– System Time
T_c	– Cycle Time
TACC	– Tactical Air Control Center
TACM	– Tactical Air Control Manual
TACS	– Tactical Air Control System
TAF	– Tactical Air Force
TAFIIS	– Tactical Air Force Integrated Information System
TCCF	– Tactical Communications Control Facility
TDMA	– Time Division Multiple Access
TG	– Transfer Grant
T/R	– Transmit/Receive
TT	– Time to Transmit 1 block of 1040 words
TTY	– Teletype
TU	– Time Unit
UER	– Undetected Error Rate
VB	– Virtual Bus
$W_{(i)}$	– Access Delay of Message $N_{(i)}$
WR	– Weighted Rating
WT	– Weight

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